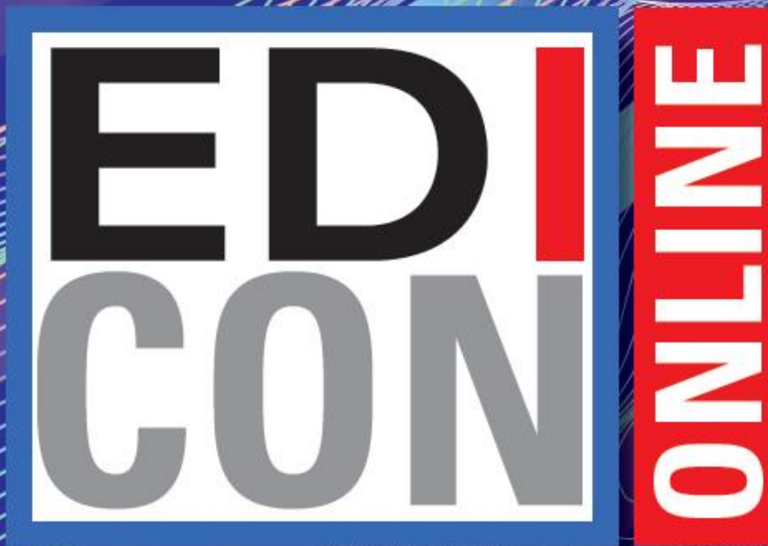
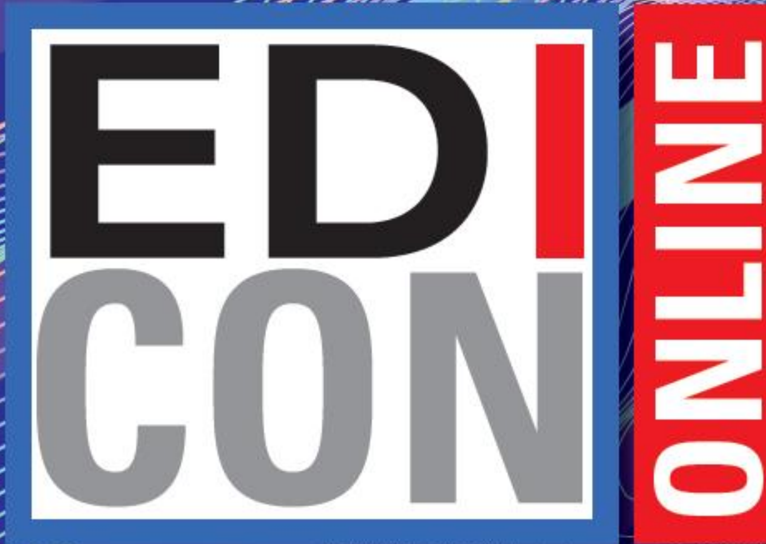


Interconnect Design for Advanced Phased Array Systems

Session Presented By: Zachariah Peterson

Date: 10/19/2022

Track: PCB/Interconnect Design



Presenter Bio

Zachariah Peterson has an extensive technical background in academia and industry. He currently provides research, design, and marketing services to companies in the electronics industry. Prior to working in the PCB industry, he taught at Portland State University and conducted research on random laser theory, materials, and stability. His background in scientific research spans topics in nanoparticle lasers, electronic and optoelectronic semiconductor devices, environmental sensors, and stochastics. His work has been published in over a dozen peer-reviewed journals and conference proceedings, and he has written 1000+ technical blogs on PCB design for a number of companies. He is a member of IEEE Photonics Society, IEEE Electronics Packaging Society, American Physical Society, and the Printed Circuit Engineering Association (PCEA), and he previously served on the INCITS Quantum Computing Technical Advisory Committee.

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Success in interconnect design for phased arrays

- PCB stackup
  - Materials (dielectrics, copper, surface plating)
  - Layer arrangement (SIG, GND, PWR, mixed on each layer…)
- Transmission lines
  - Coplanar, microstrip, or stripline
- Via design
  - Very important in dense phased arrays

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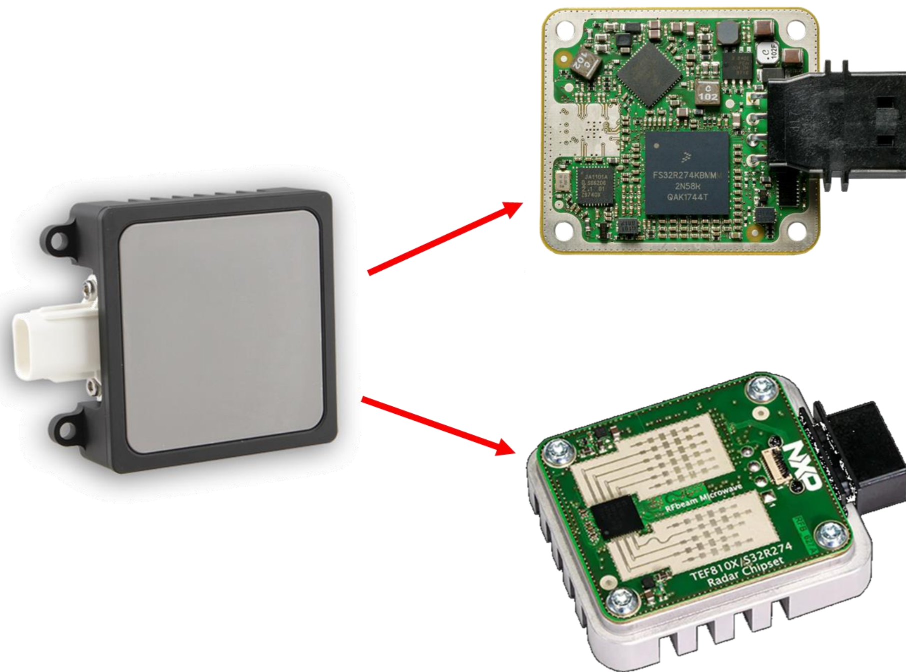
Success in interconnect design for phased arrays

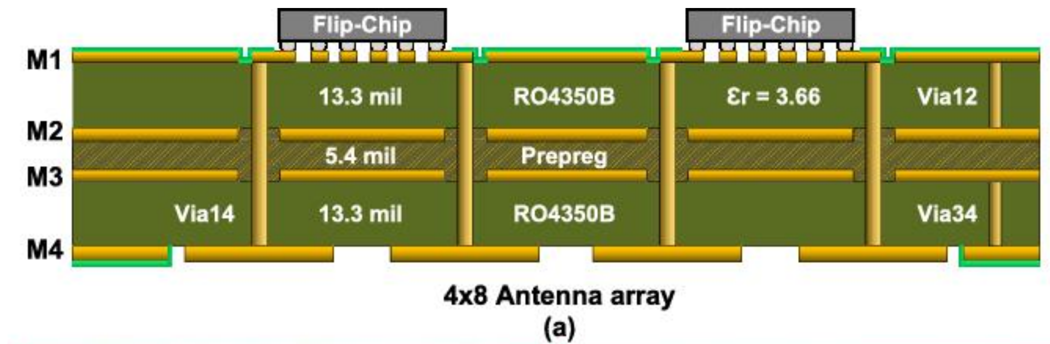
- Beamforming type
  - Analog, digital, or hybrid?

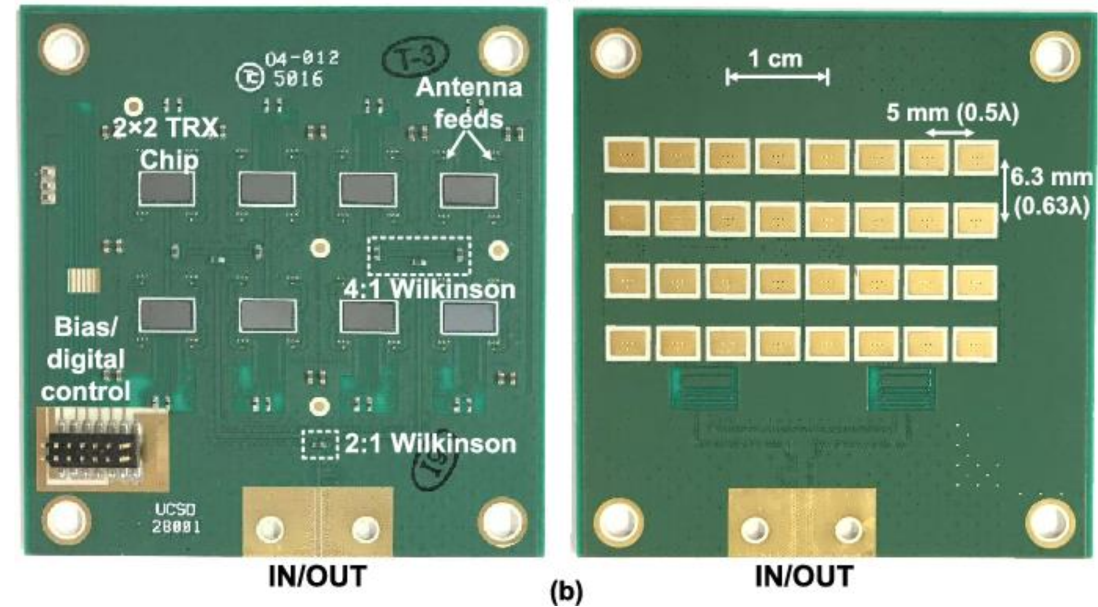
- Antenna co-location
  - Not rigorously defined
  - Needed to determine resolution

More Emitters, Higher Density

- Trend towards larger arrays
  - More elements = higher resolution
  - More elements = higher gain
  - More elements = more users via spatial multiplexing (MU-MIMO)



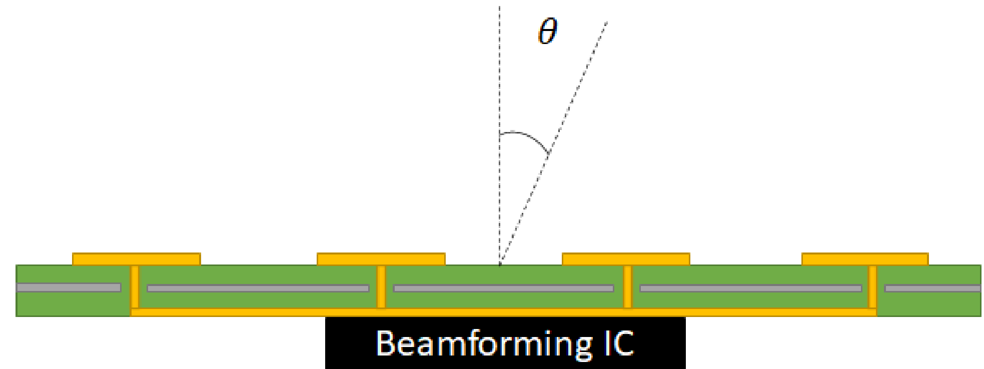


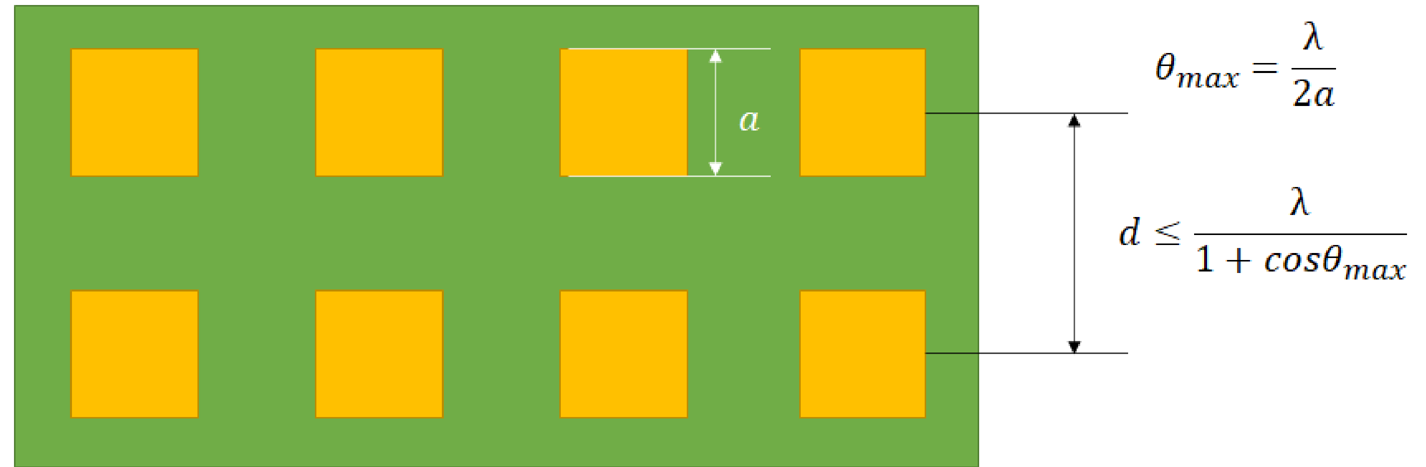


Analog Beamforming

- Requires phase matching, or known phase mismatch that is compensated

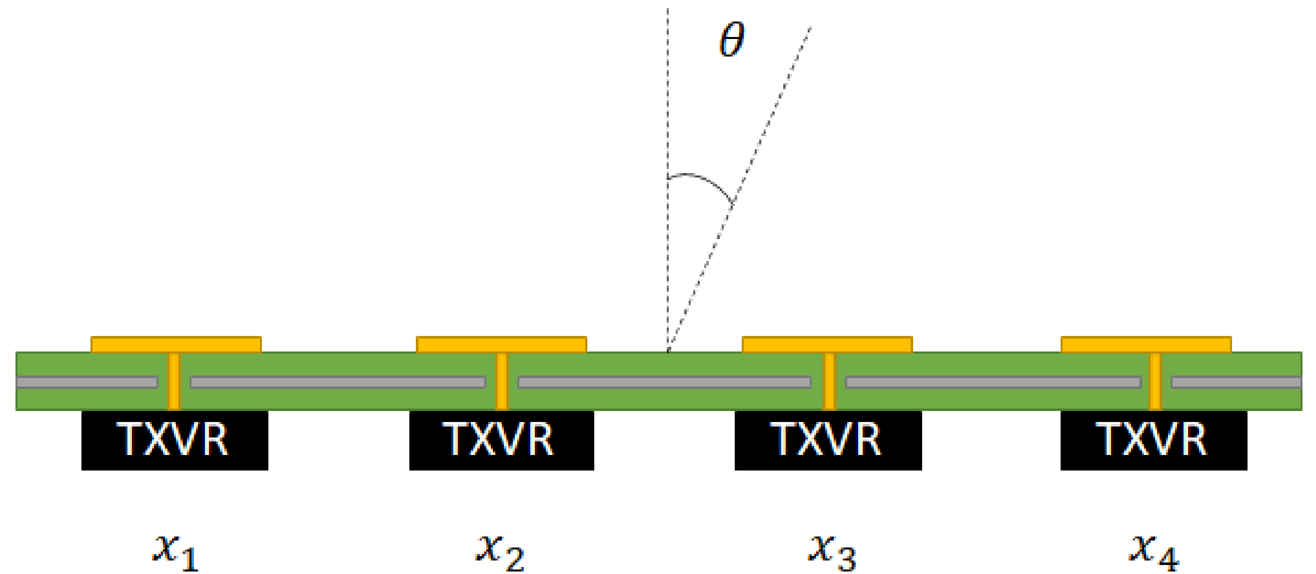
- Emission pattern controlled with phase





Digital Beamforming

- Requires mixing amplitudes and phases of incoming bitstreams
- Easier to compensate known phase mismatch
- More scalable?



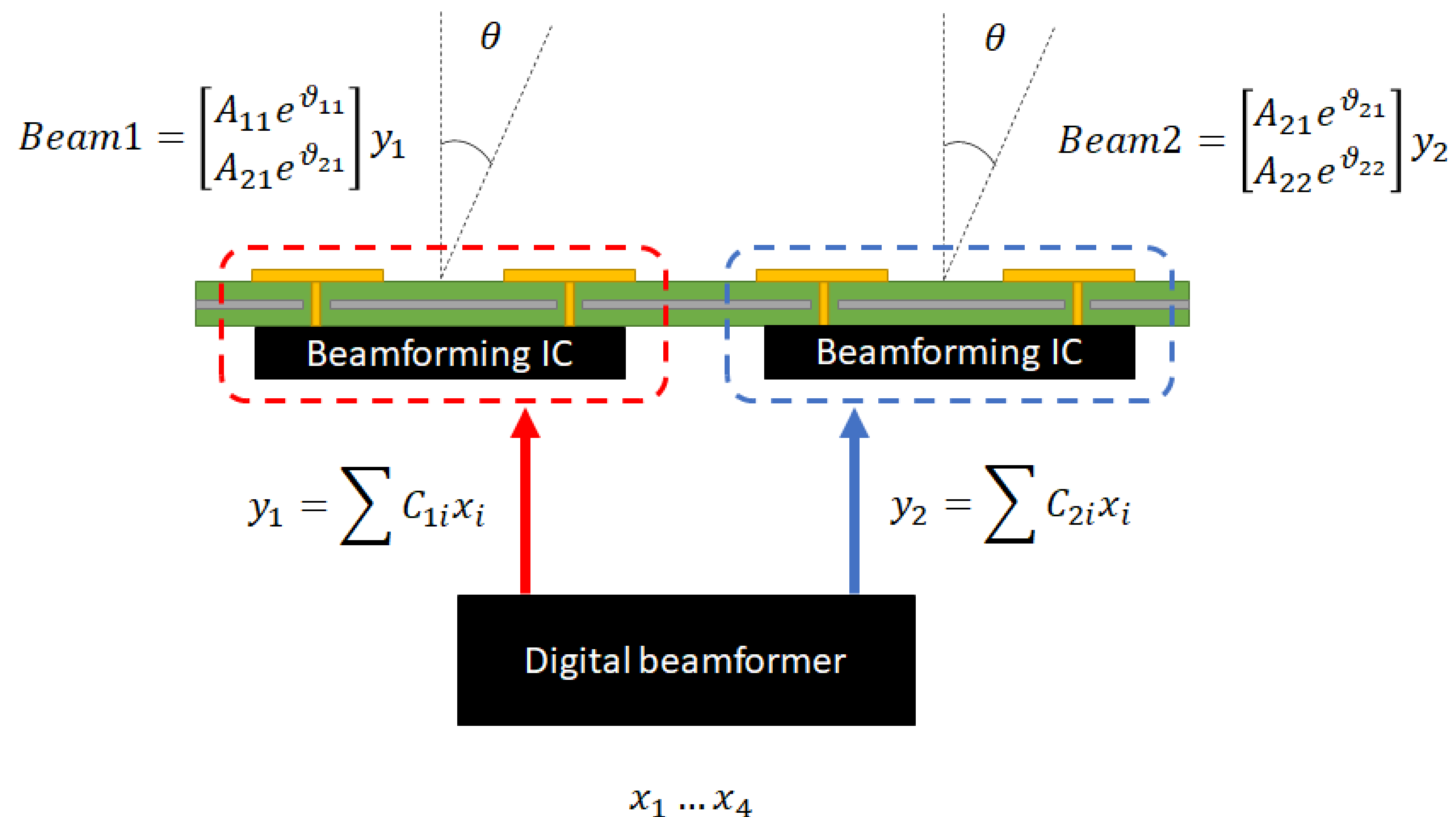
$$Y(\vec{\boldsymbol{r}}, \omega) = \sum y_i(\omega, \varphi) A_i(\vec{\boldsymbol{r}})$$

$$\begin{bmatrix} y_1 \\ \vdots \\ y_N \end{bmatrix} = \begin{bmatrix} C_{11} & \cdots & C_{1N} \\ \vdots & \ddots & \vdots \\ C_{N1} & \cdots & C_{NN} \end{bmatrix} \begin{bmatrix} x_1 \\ \vdots \\ x_N \end{bmatrix}$$

Hybrid Beamforming

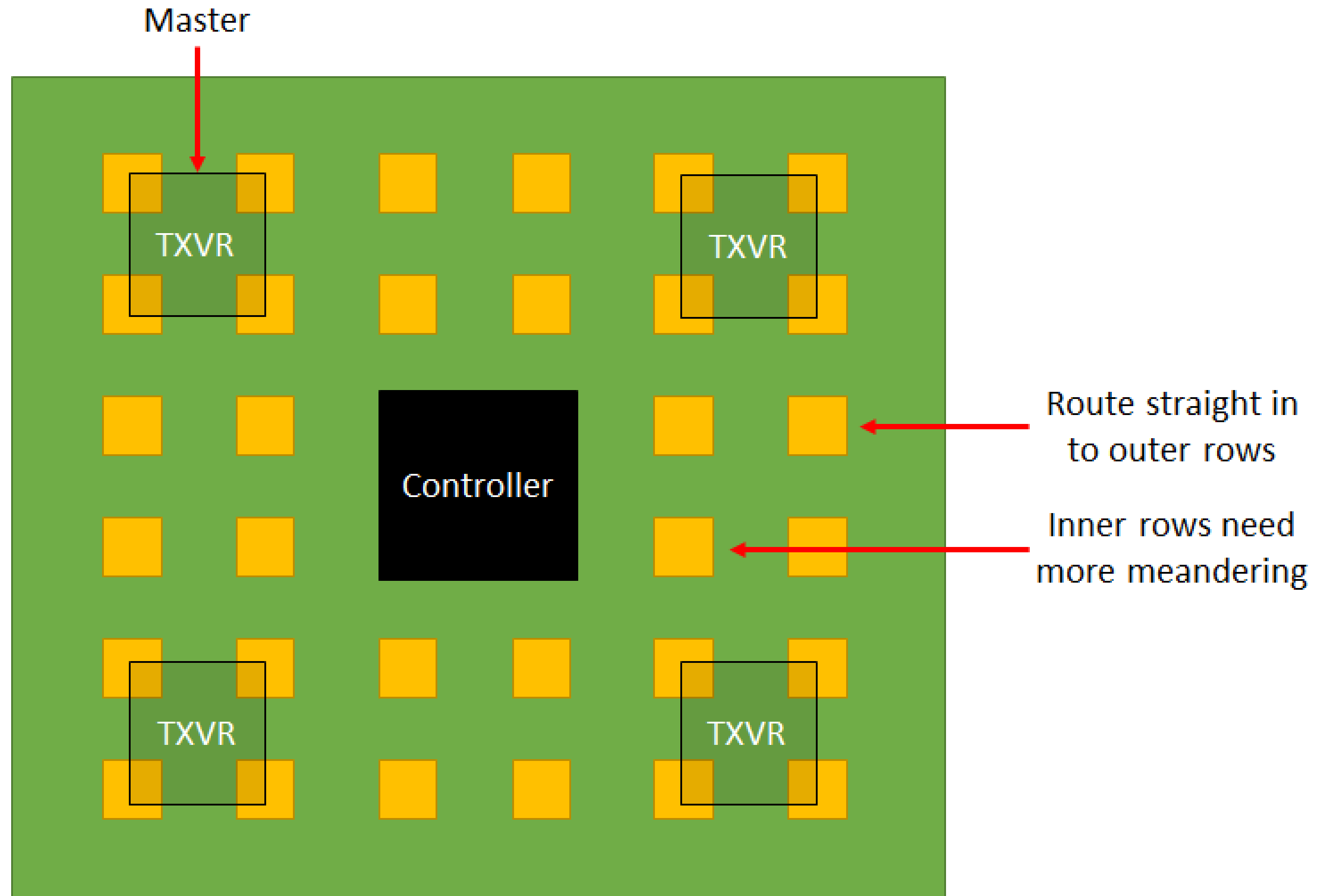
- Requires mixing amplitudes and phases of incoming bitstreams

- Emission constructed through phase control in each beamforming IC



Example Layout Concept

- GCPW's on back layer
- Control signals on internal layers
- Power on internal layer (multiple rails in general)



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Transmission Line Theory: RLCG model

- TL characteristic impedance: $Z_0 = \sqrt{\frac{R+i\omega L}{G+i\omega C}}$

$$R(\omega) = R_{DC} + \sqrt{\omega} R_s \qquad L(\omega) = L_\infty + R_s / \sqrt{\omega}$$

Incomplete

$$G(\omega) = \omega C(\omega) \tan\delta(\omega) \qquad C(\omega) = K_g \varepsilon_R(\omega) \varepsilon_0$$

- Dielectric constant: $\varepsilon = \varepsilon_R(\omega) + i\varepsilon_I(\omega), tan\delta = \frac{-\omega\varepsilon_I(\omega) - \sigma_{sub}}{\omega\varepsilon_R}$
- Need causal models or data for:

Dielectric constant: $\varepsilon(\omega)$

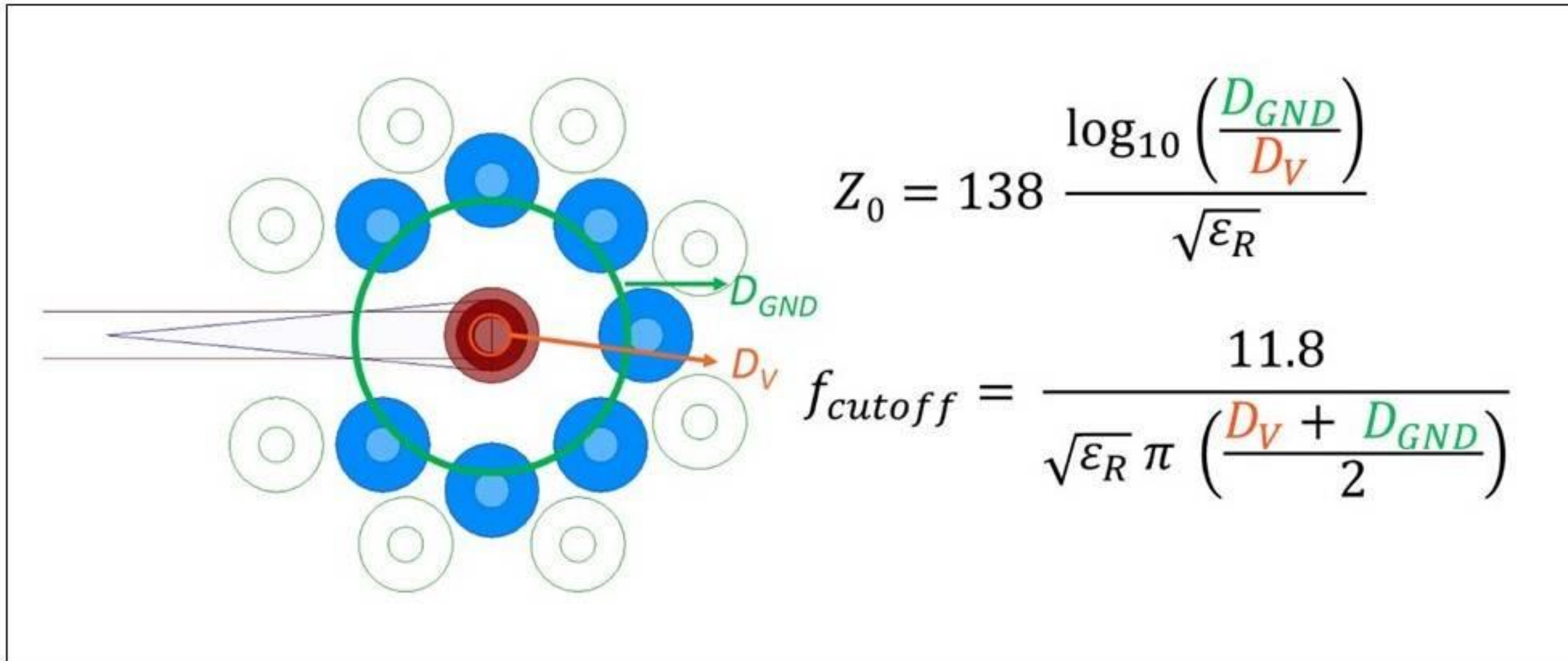
Copper roughness: $K(\omega)$

Electrical parameters: $R(\omega), L(\omega)$

Zhang, J., et al. "Causal RLGC(*f*) Models for Transmission Lines From Measured *S*-Parameters," *IEEE Transactions on Electromagnetic Compatibility*, 52(1), pp.189-198 (2009).

Wideband Signal Launch

- Connector/component launches into a signal via



f in GHz, D_V, D_{GND} in inches

Boesing, D. "Maximizing RF Launch Performance: The Impact Of GND Vias." Samtec.

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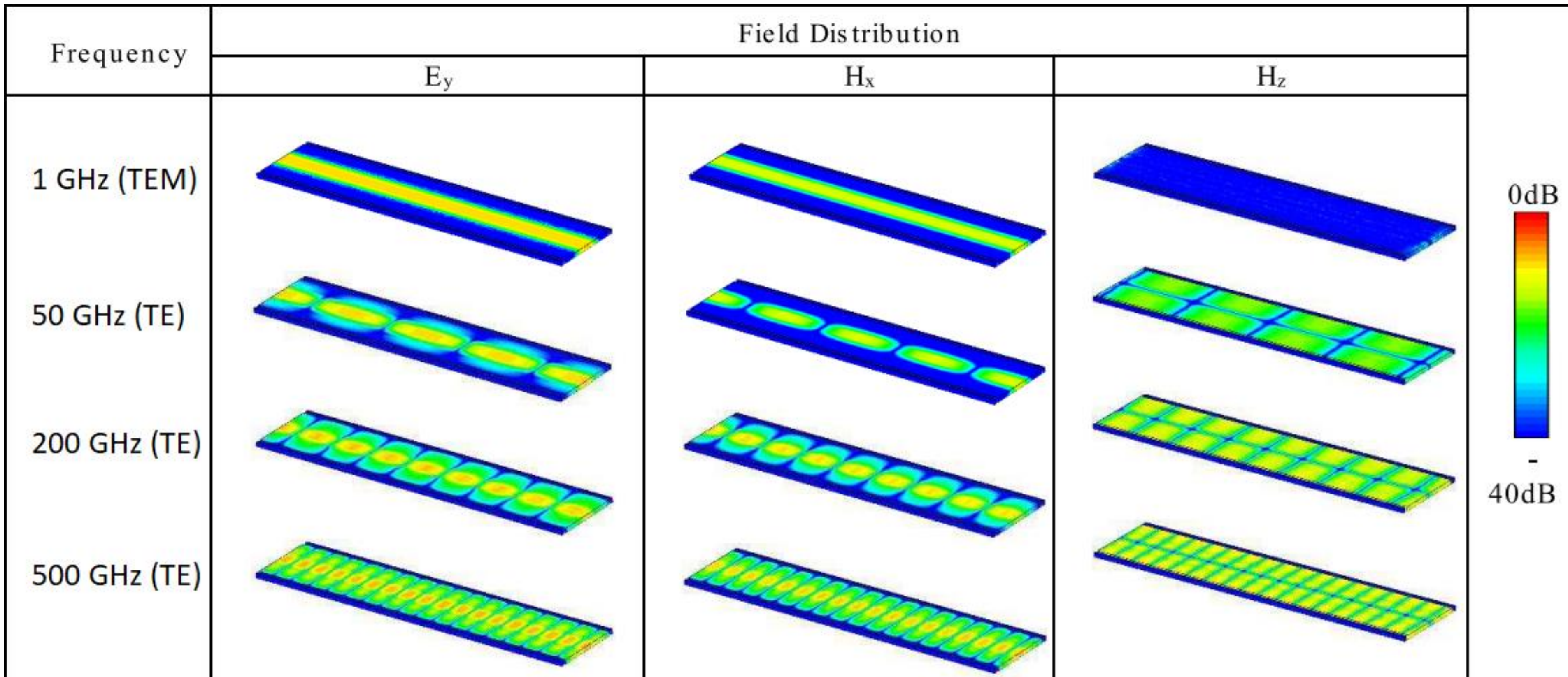
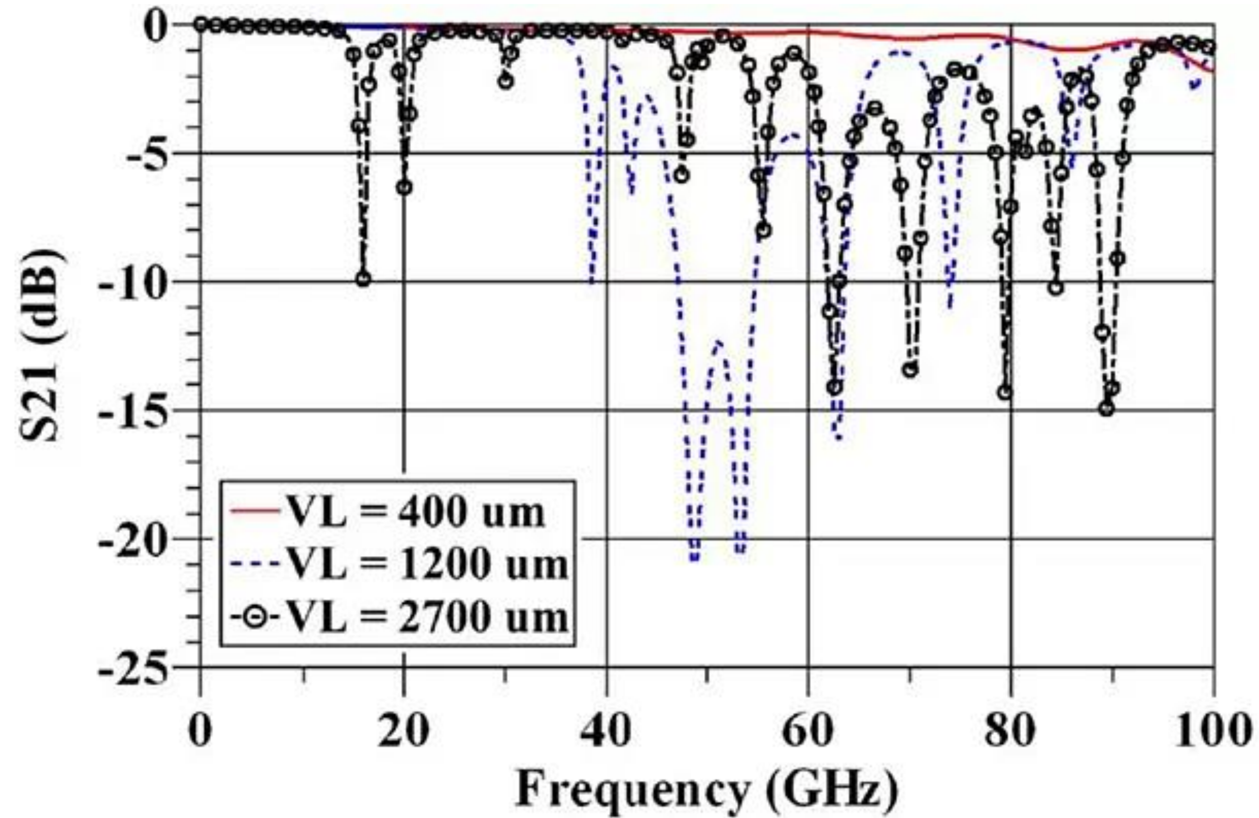
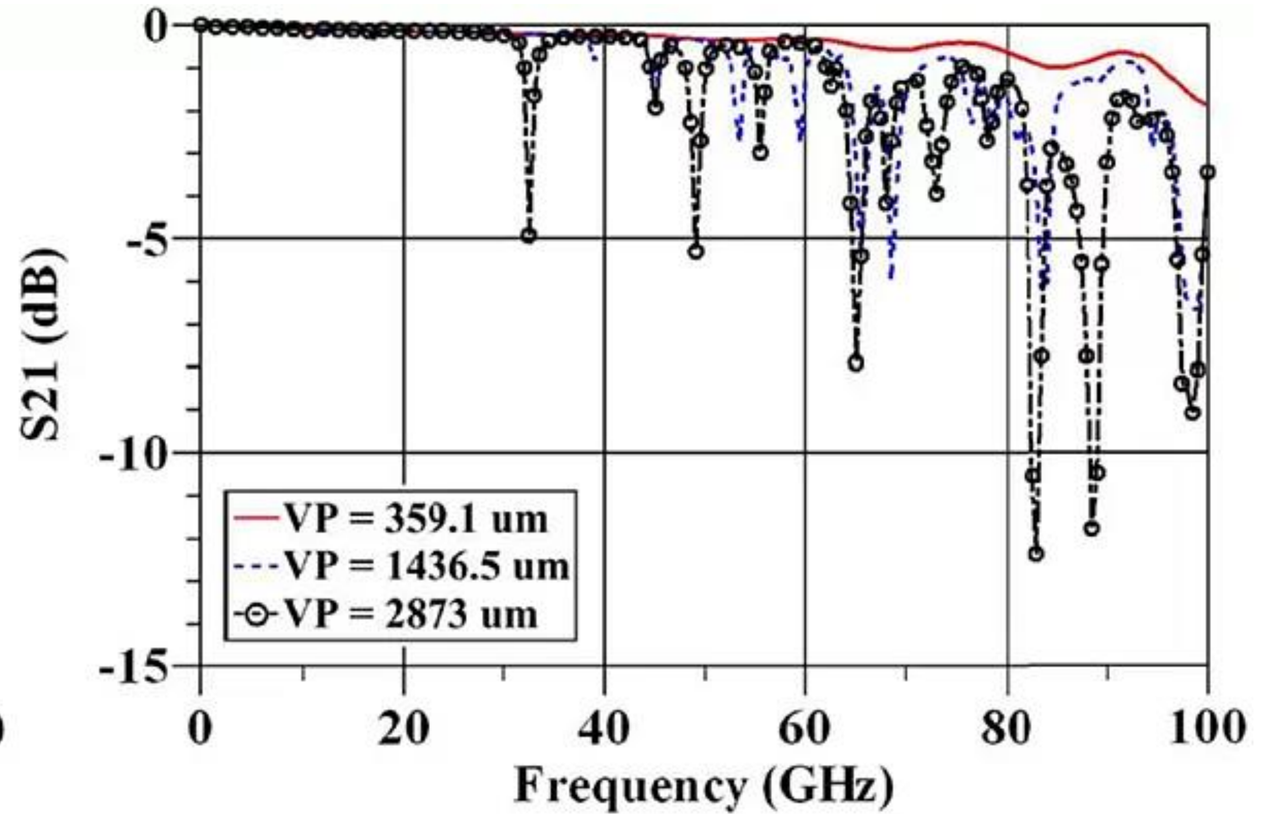
Coplanar Waveguides



Fesharaki, Faezeh, Tarek Djerafi, Mohamed Chaker, and Ke Wu. "Guided-wave properties of mode-selective transmission line." *IEEE Access* **6** (2017): 5379-5392.

Coplanar Waveguides

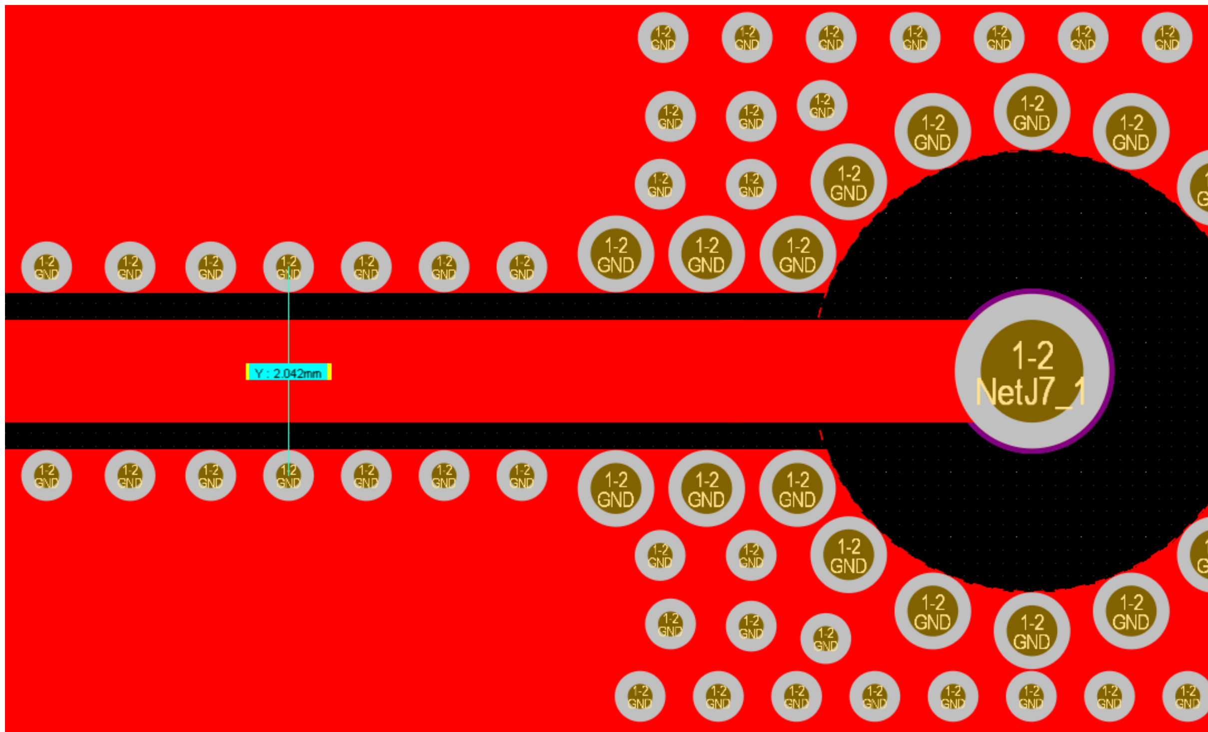


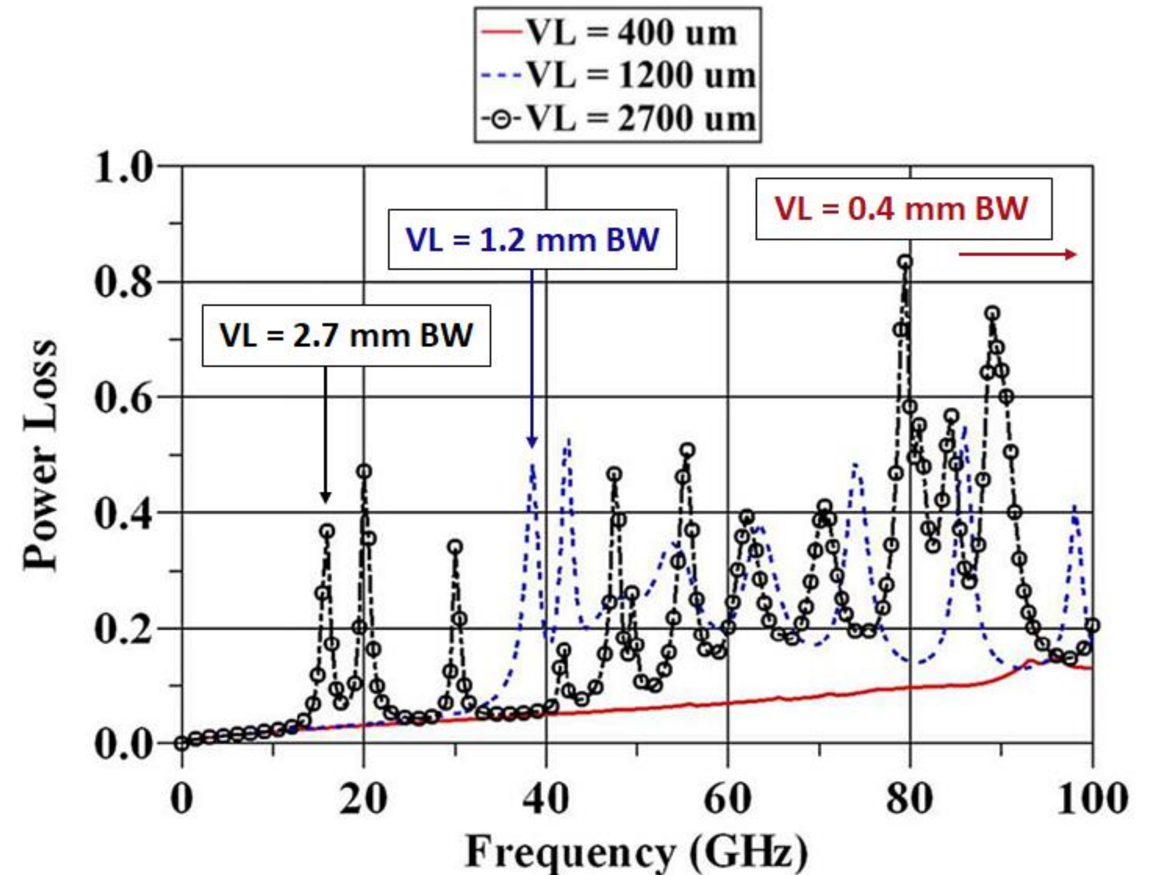


Sain, Arghya, and Kathleen L. Melde. "Impact of ground via placement in grounded coplanar waveguide interconnects." *IEEE Transactions on Components, Packaging and Manufacturing Technology 6*, no. 1 (2015): 136-144.

Coplanar Waveguides

- Example: 2.042 mm via spacing on 30 mil RO4350B
  - →50 Ohm impedance up to 42 GHz





Sain, Arghya, and Kathleen L. Melde. "Impact of ground via placement in grounded coplanar waveguide interconnects." *IEEE Transactions on Components, Packaging and Manufacturing Technology* 6, no. 1 (2015): 136-144.

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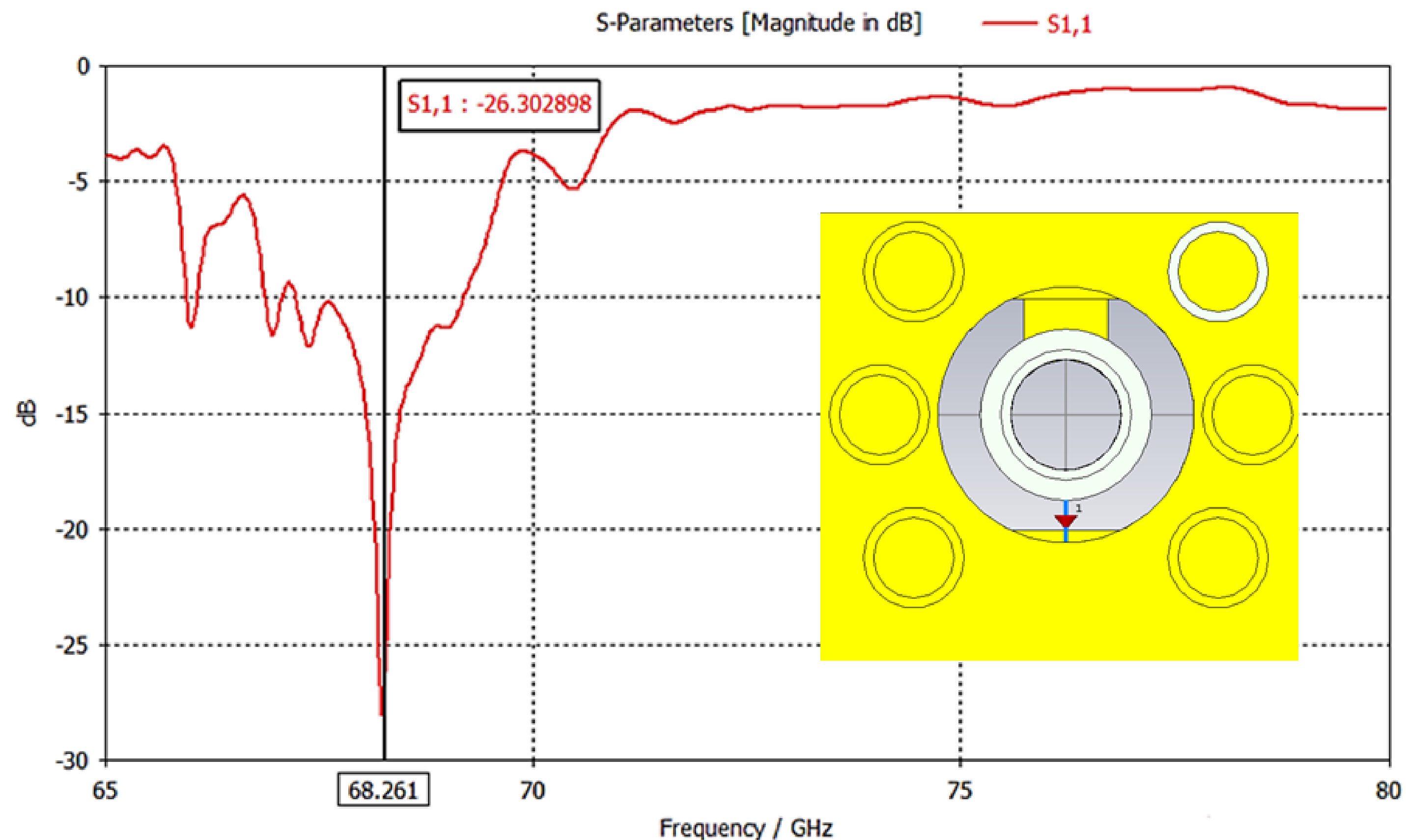
Via Transitions

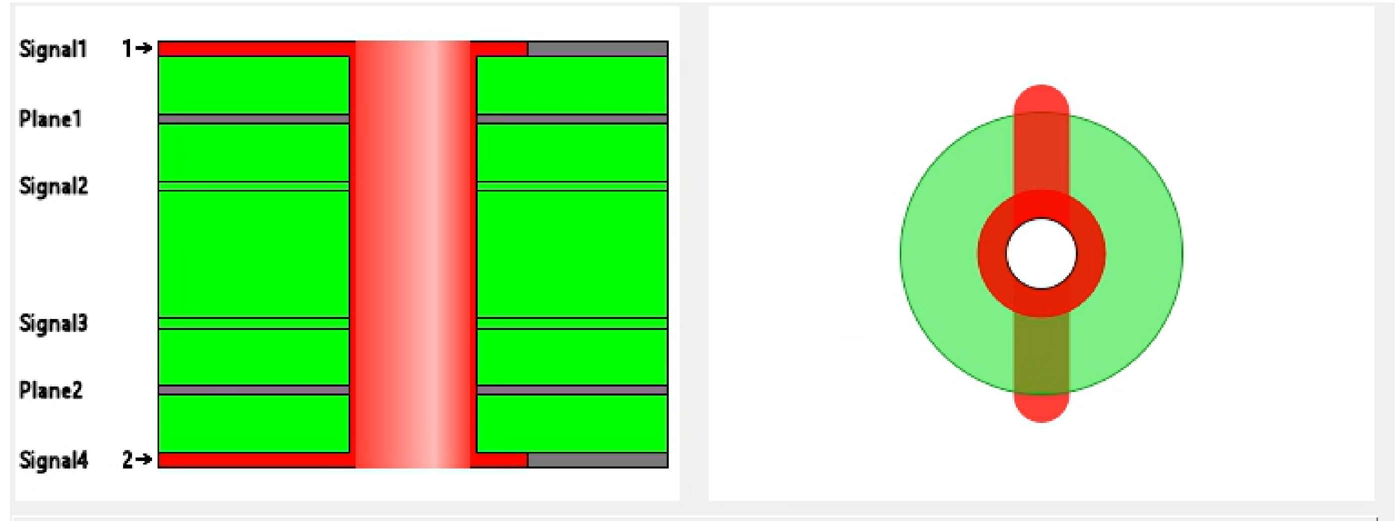
- ***Most via impedance calculators are incomplete***

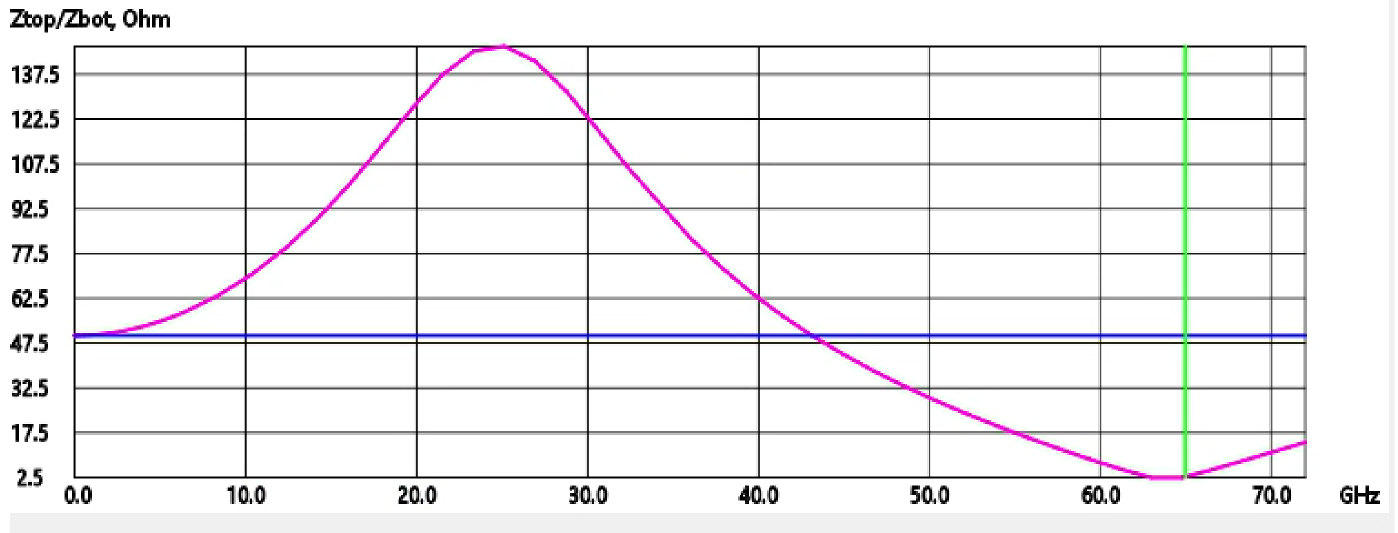
- Need to design:
  - Via dimensions
  - Pad + antipad size
  - Remove or keep NFPs?
  - Stitching vias required at high frequency to hit 50 Ohms



Effect of Stitching Vias

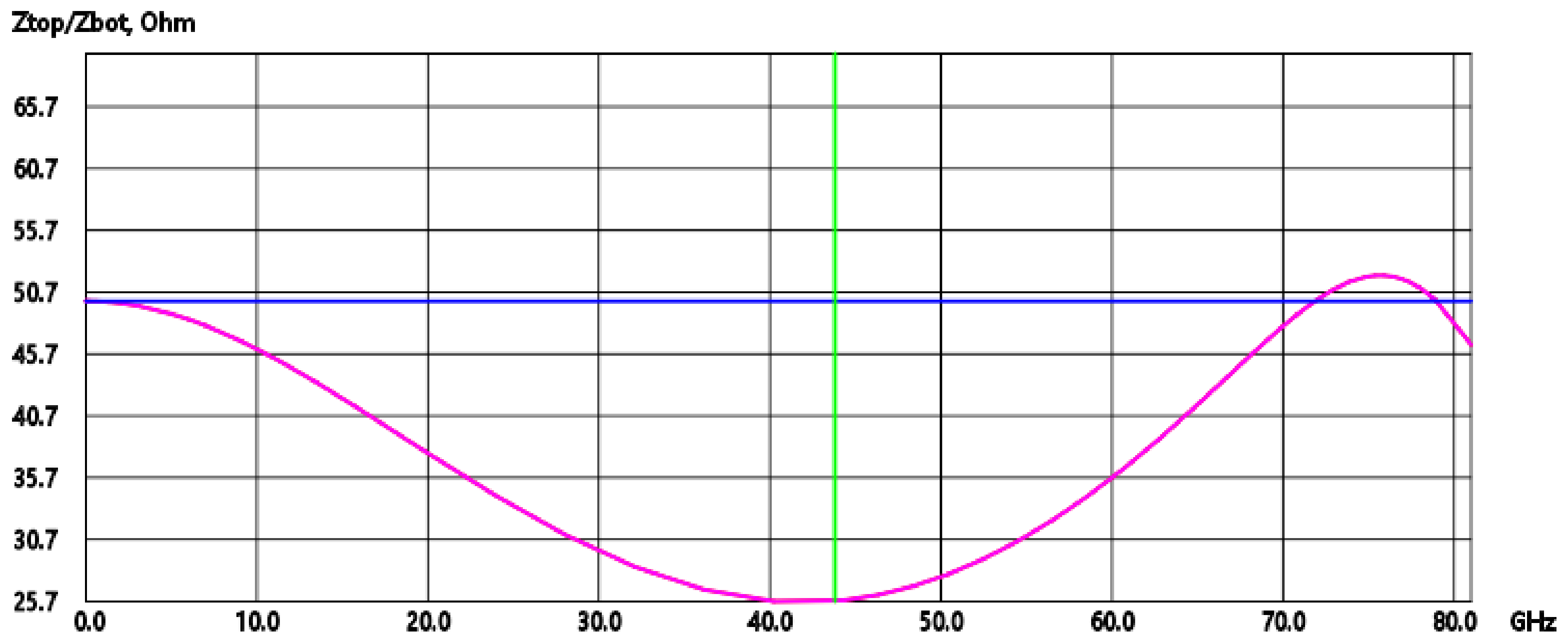
- Via impedance with no stitching vias → initially inductive, then capacitive

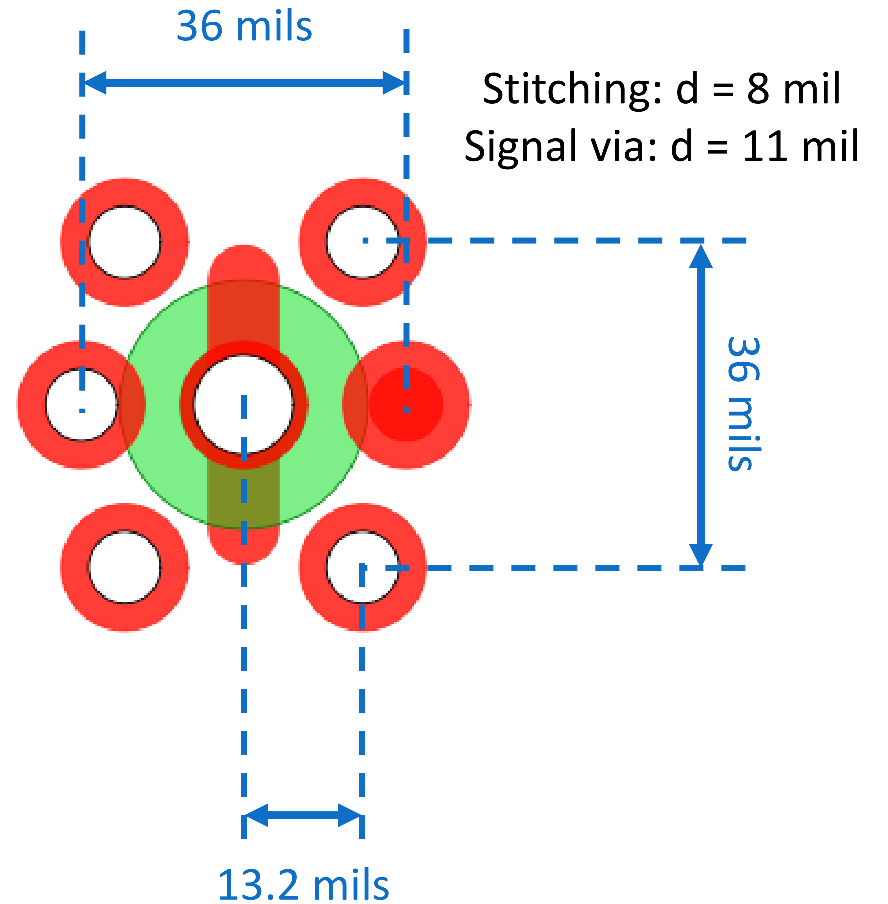




Effect of Stitching Vias

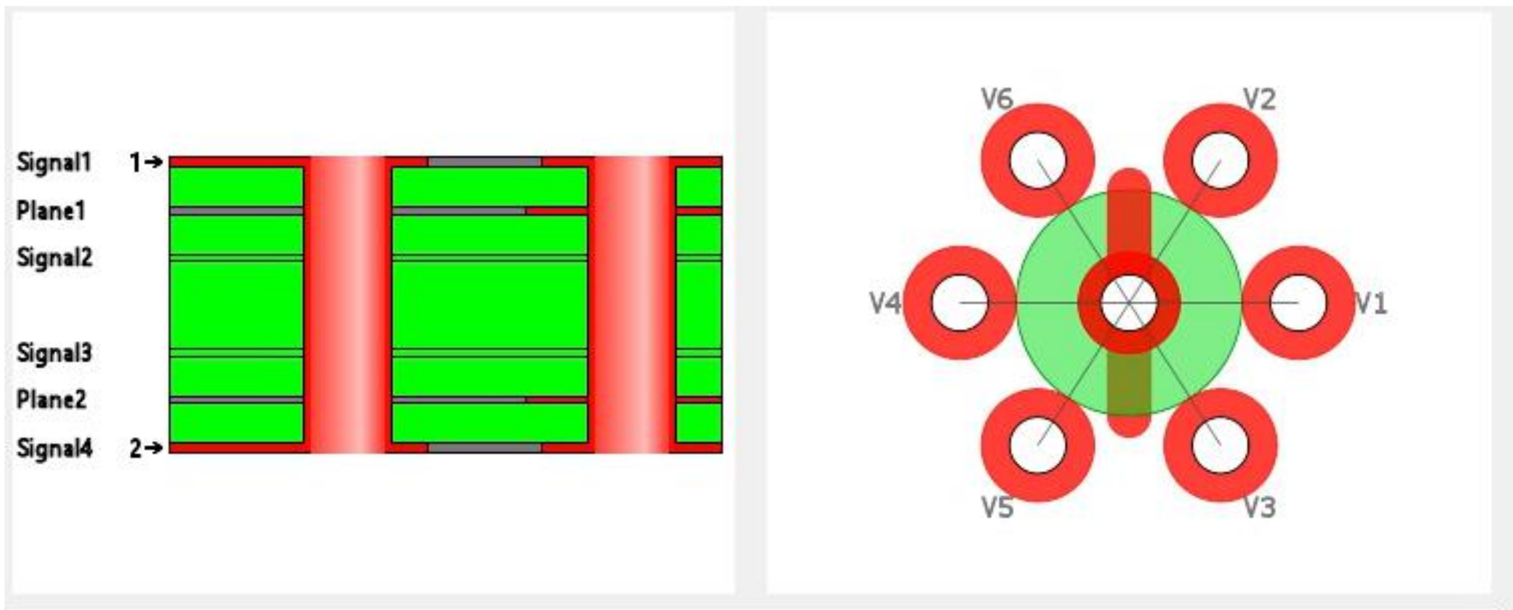
- Via impedance with stitching vias → can appear capacitive, then inductive
- Getting to the limit of manufacturing capabilities

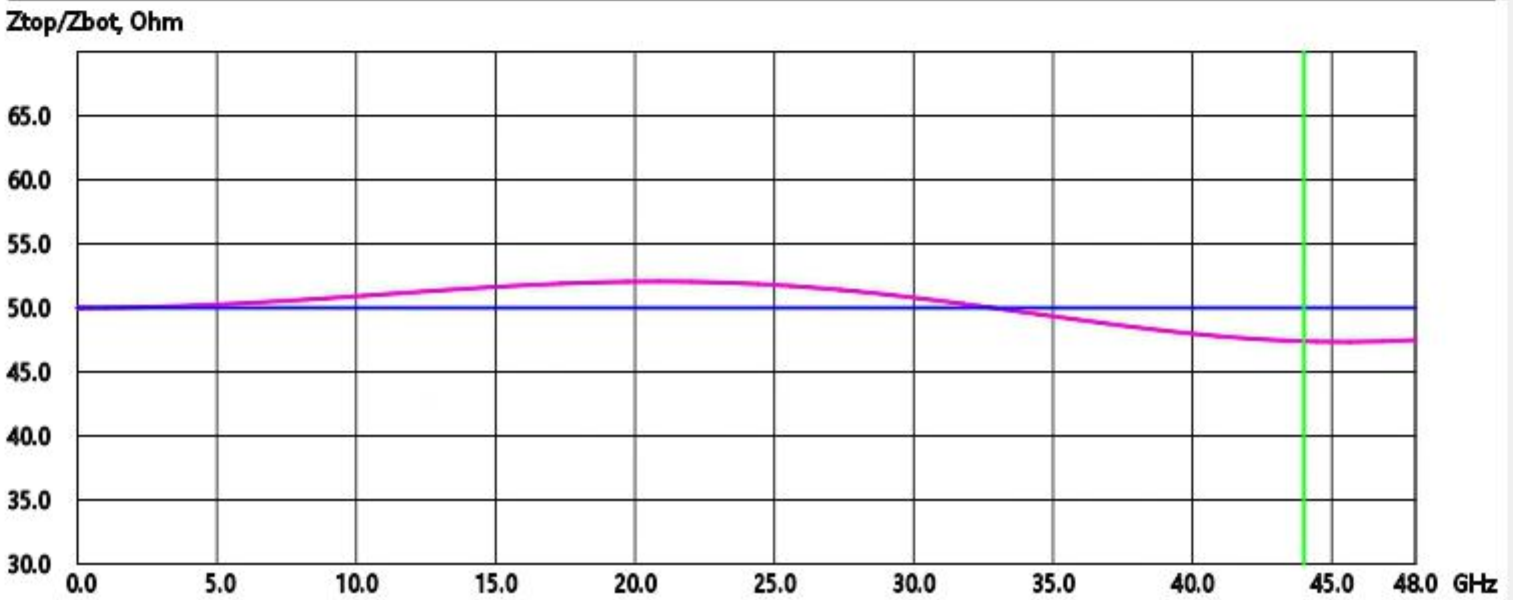




Ideal result

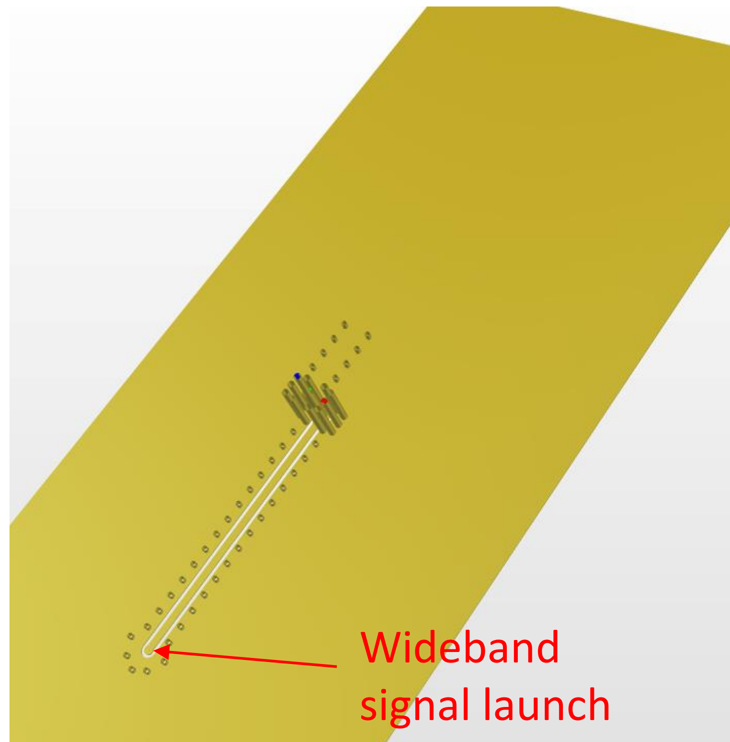
- Very broad bandwidth signal transition matched near 50 Ohms
- Longer vias sometimes better than shorter vias!
  - → Due to capacitive loading @ pad region
  - Aim for higher impedance

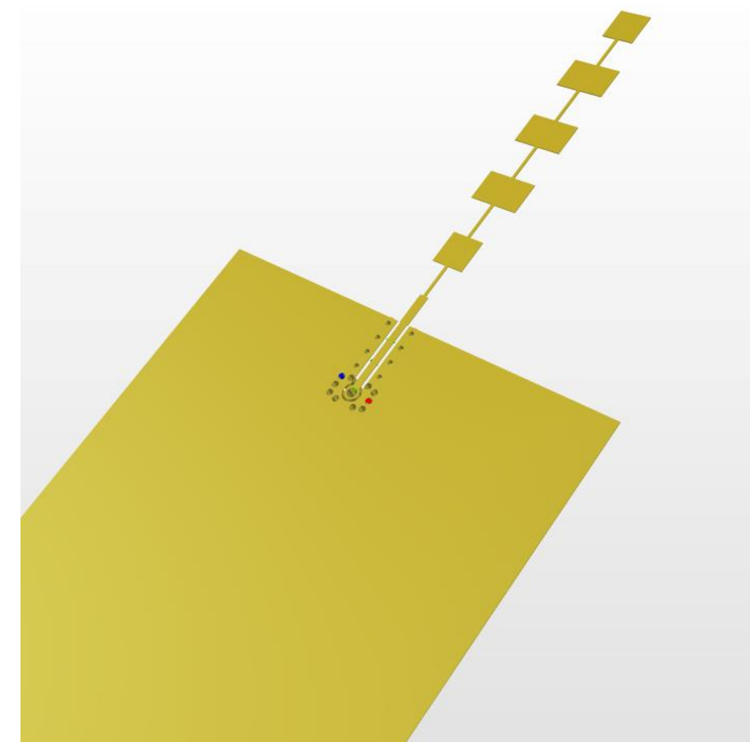




Narrowband (Via + Feedline) Interconnect

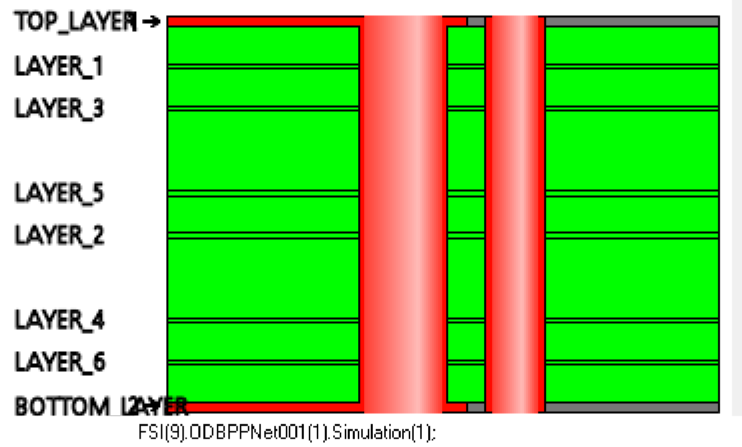
- Should the via transition directly to the antenna, or should there be a short section of feedline?
- Hybrid stackup, 8 layers
- 1-λ transformation, low loss → input impedance at via evaluates to $Z_{in} \approx \frac{Z_L Z_0}{Z_0} \approx Z_L$

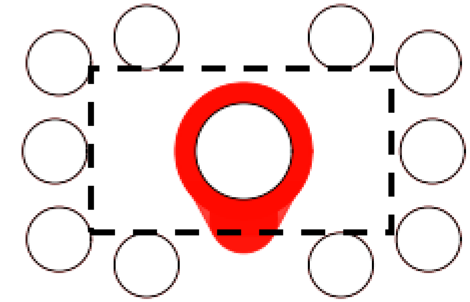




Examples With Via + Feedline

12/17 mil center via
8 mil stitching vias
100 mil top feedline
~9 ps delay





DBMagnitude(S), [dB]

0
-5
-10
-15
-20
-25

72.93 GHz

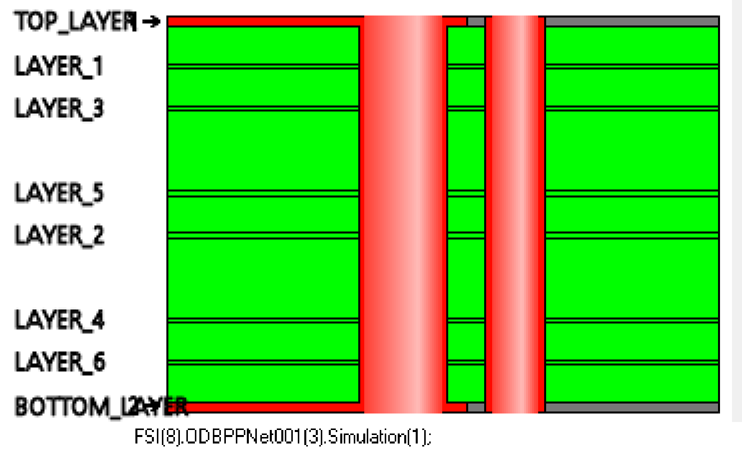
71.5 72 72.5 73 73.5 74 74.5 75 75.5 76 76.5 77 77.5 78 78.5 79 79.5 80 80.5 81 81.5 82

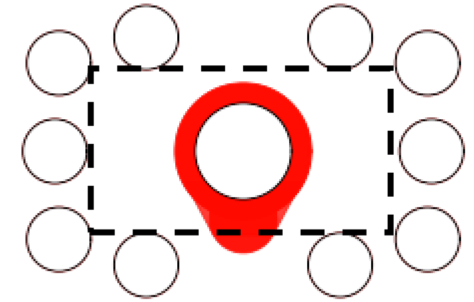
Frequency, [GHz]

S[1,1];

Examples With Via + Feedline

12/17 mil center via
8 mil stitching vias
96.382 mil top feedline
~9 ps delay





FSI(8).ODBPPNet001(3).Simulation(1);

DBMagnitude(S), [dB]

-2.5
-5
-7.5
-10
-12.5

77.03 GHz

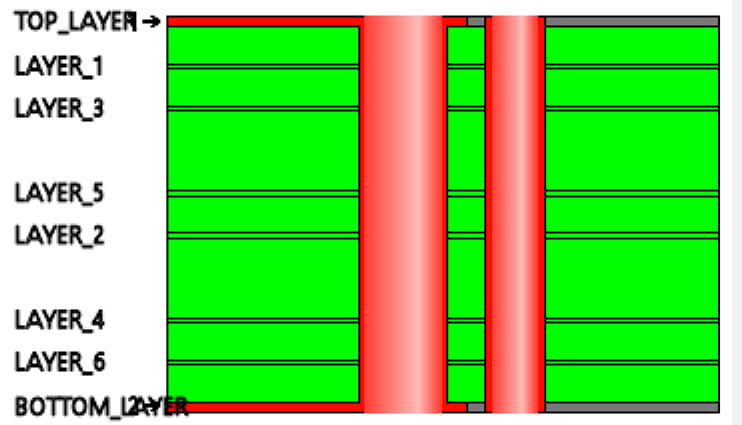
71.5 72 72.5 73 73.5 74 74.5 75 75.5 76 76.5 77 77.5 78 78.5 79 79.5 80 80.5 81 81.5 82

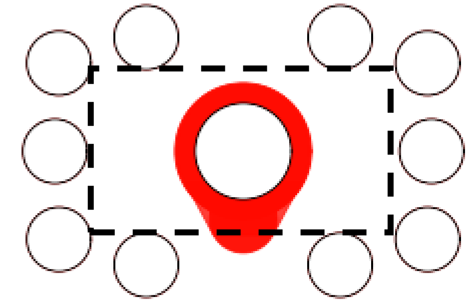
Frequency, [GHz]

S[1,1];

Examples With Via + Feedline

12/17 mil center via
8 mil stitching vias
94.71 mil top feedline
~9 ps delay

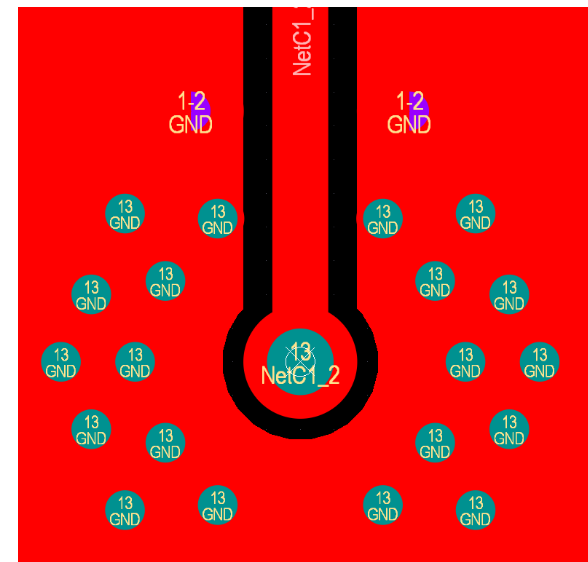




More Stitching Vias

10/17 mil center via
6 mil stitching vias
96.382 mil top feedline
~9 ps delay
Circular annular ring

More vias = Better matching, higher Q



FSI(1).ODBPPNet001(1).Simulation(1);

DBMagnitude(S), [dB]

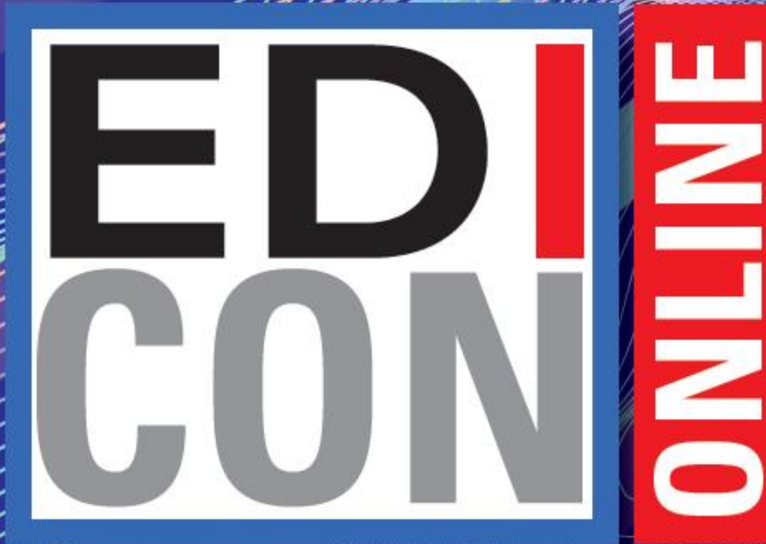
-5
-10
-15
-20

71.5 72 72.5 73 73.5 74 74.5 75 75.5 76 76.5 77 77.5 78 78.5 79 79.5 80 80.5 81 81.5 82

Frequency, [GHz]

77.179 GHz

S[1,1];



Conclusion

- Signal launches typically use blind vias, but scalable phased arrays might require through-holes
- Can use cables/connectors between boards, but eliminate these to get a compact system
- Wideband through-hole via design into the many-GHz range is a persistent challenge