



# PCB Design Optimization: What it Means and New Methods

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# INTRODUCTION

- What is PCB design optimization?
  - **Marketing speak!**

Our product optimizes performance enhancement while mitigating degradation to optimized improvements...

# INTRODUCTION

- **Optimization:** An important area of engineering and design
- All design engineers do optimization subconsciously:
  - **Finding tradeoffs in a design**
  - **Balancing tradeoffs**
- **Mathematically:** Maximize/minimize something subject to some constraints

# What is PCB Design Optimization?

- Mathematical definition:

Max. or min.  $f(x_1, x_2, \dots, x_N)$

My design goal

- Impedance
- S-parameters
- Routing density
- Dispersion

Subject to:

$$\begin{aligned} g_1(x_1, x_2, \dots, x_N) &\leq A \\ g_2(x_1, x_2, \dots, x_N) &\leq A \\ &\vdots \end{aligned}$$

My constraints

- Any design goal could be a constraint

$$|x_1, x_2, \dots, x_N| \leq C$$

My design variables

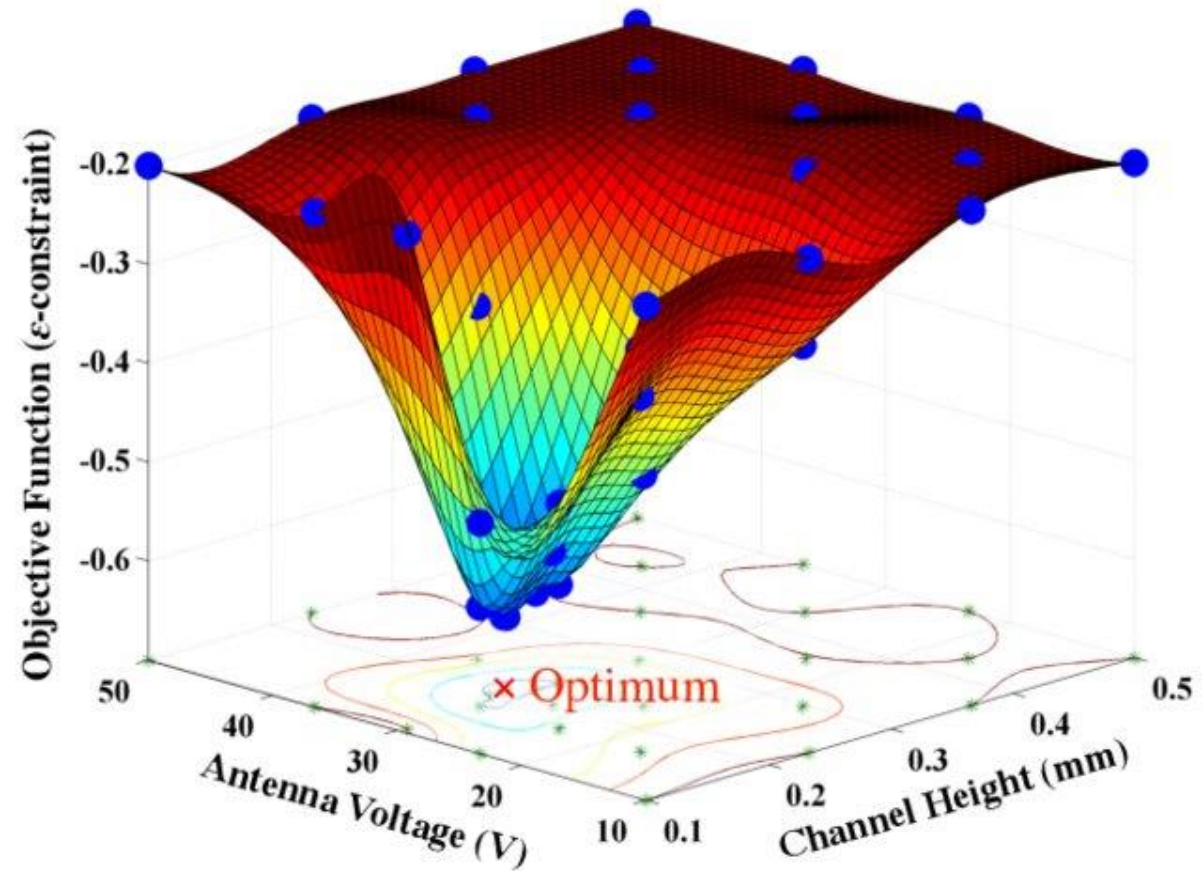
- Usually geometric

- How to choose  $x_1, x_2, \dots, x_N$  so that I meet my objective function

$f(x_1, x_2, \dots, x_N)$  while satisfying  $g_1, g_2, \dots$

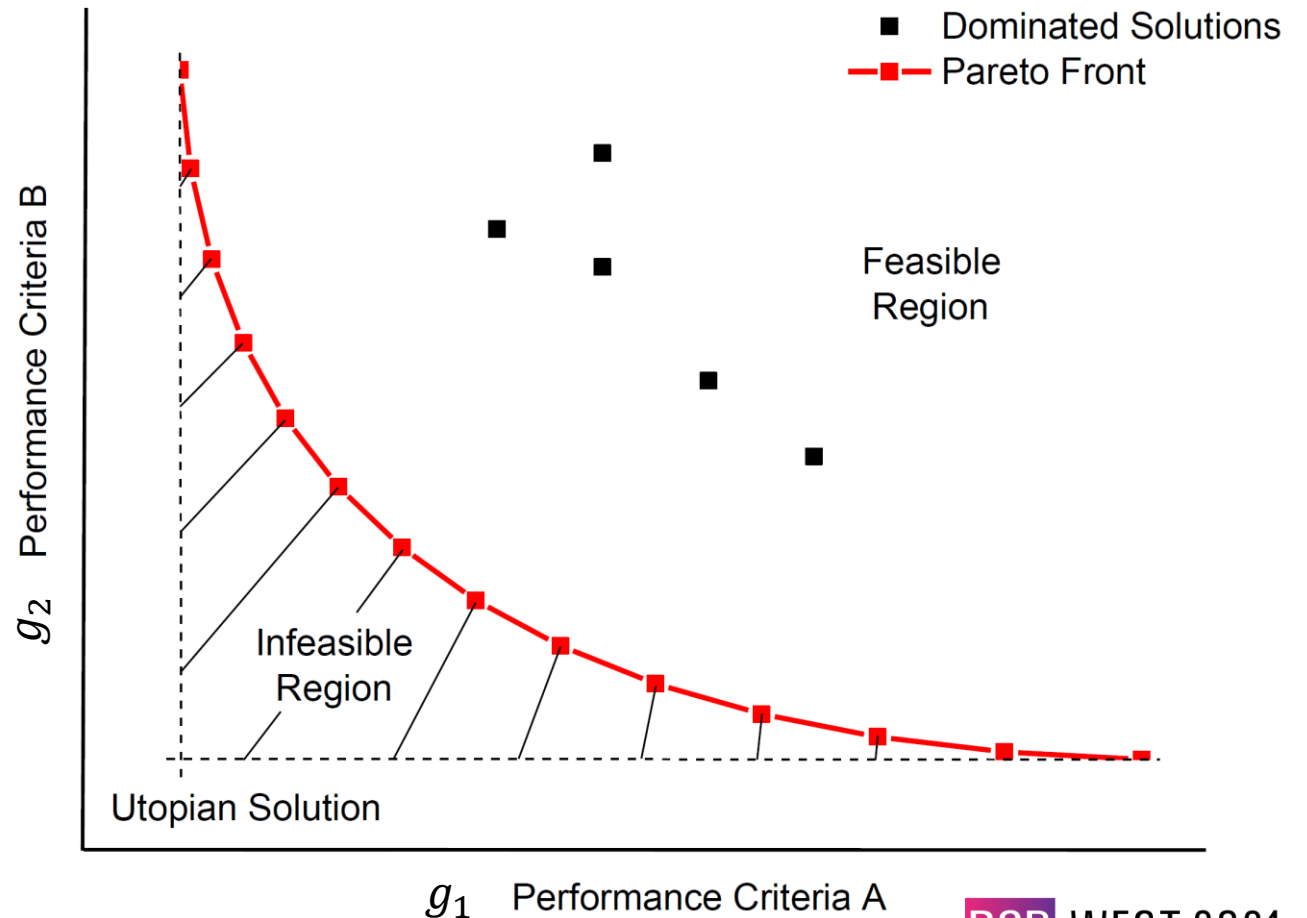
# Optimization = Analyzing Tradeoffs

- All engineering problems are optimization problems
- Single objective = usually\* easy to get an optimum design



# Optimization = Analyzing Tradeoffs

- Real problems = multiple objectives = complex tradeoffs
- Impossible to get a “perfect” design
- More objectives = longer computation time, more difficult to visualize



# Why Worry About Design Optimization?

- **Motivation:** Newer signaling standards demand design techniques that are optimization problems
- **Motivation (II):** Designs are more complex → Way to balance great complexity

# Methods

- **Empirical**
  - Use models extracted from experimental data
- **Numerical**
  - Use simulation tools (field solvers)
- **Analytical**
  - Use equations derived from first principles → direct calculations
- Build a “catalog” of possible designs, pick the best for your system



# Empirical Methods

- **Involves measurements**

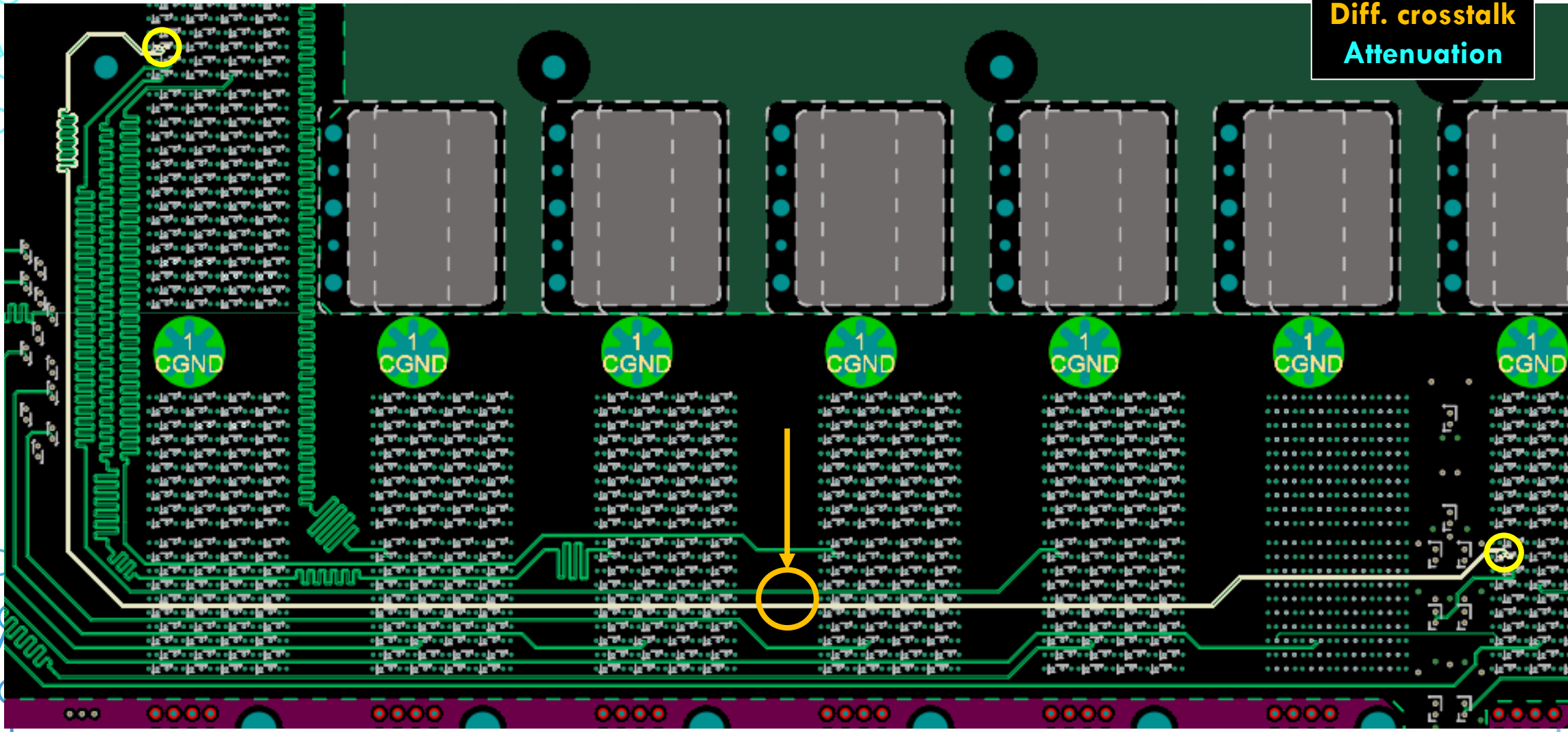
- Objective function: Signal integrity (S-parameters), impulse response
- Design variables: Channel geometry
- Parameters: Roughness, Dk/Df, stackup, via count, ...

- **Procedure:** Vary design variables, measure objectives, compare with reference model

- **Drawbacks:** Considers entire interconnect (good and bad!)

- Example with 56G channels on Eurocard backplane (6U)

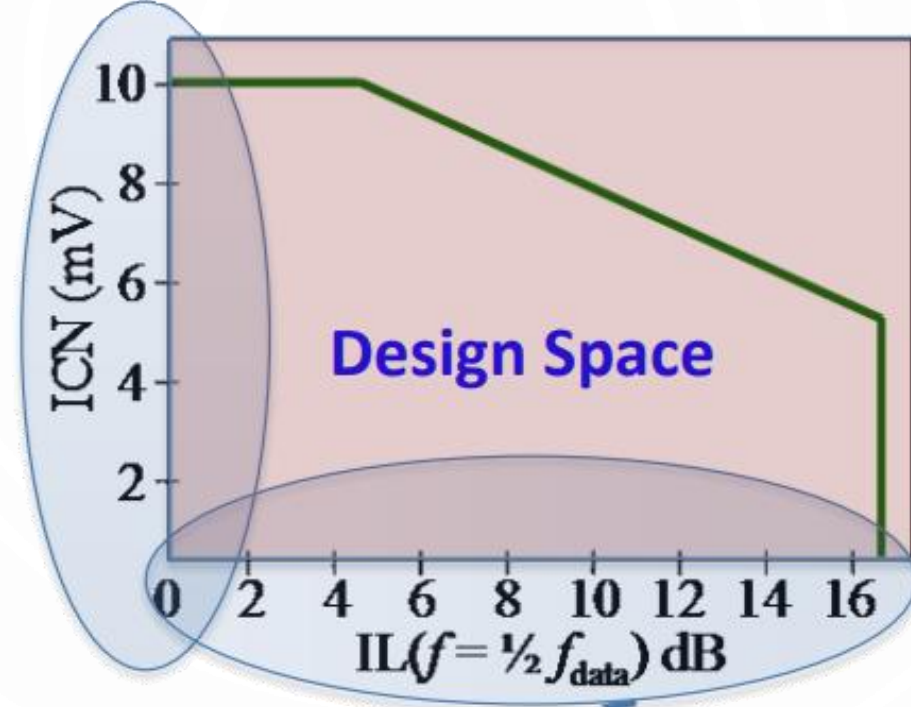
Reflections  
Diff. crosstalk  
Attenuation



• Neves et al. "Pathological Design", 100GBase-KR



**Crosstalk Noise Test vehicle, calculated RX noise as Integrated Crosstalk Noise (ICN)**



**Insertion Loss Test Vehicle (IL) at Nyquist Sampling Freq**



- **Example: Tri-objective problem in 100GBase-KR or USB 4.0**
- Uses Multi-port S-parameters for differential pair design:

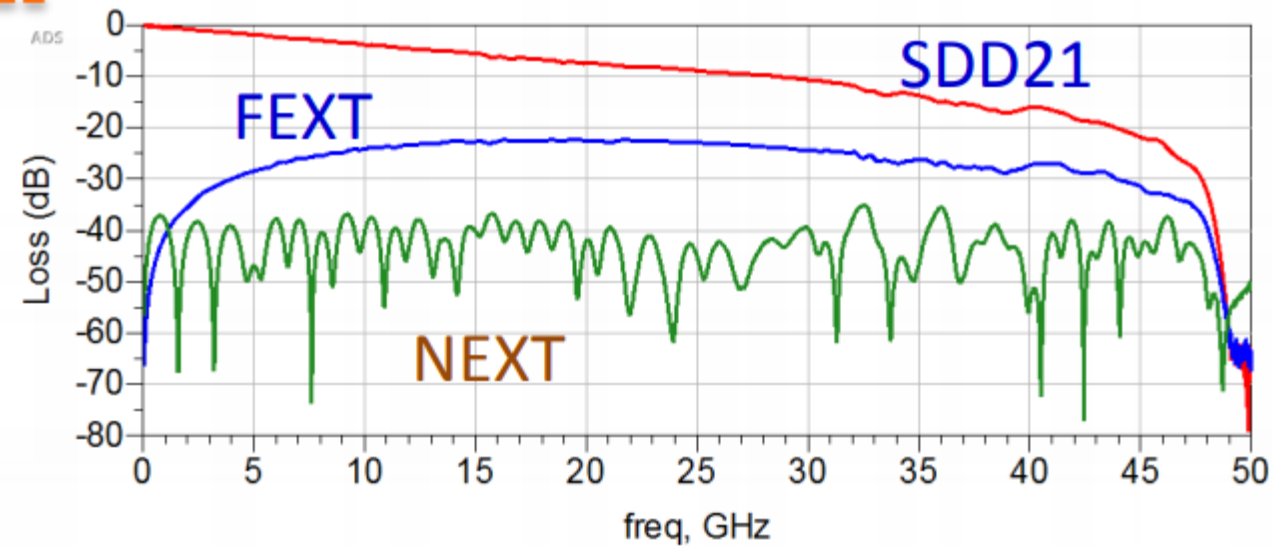
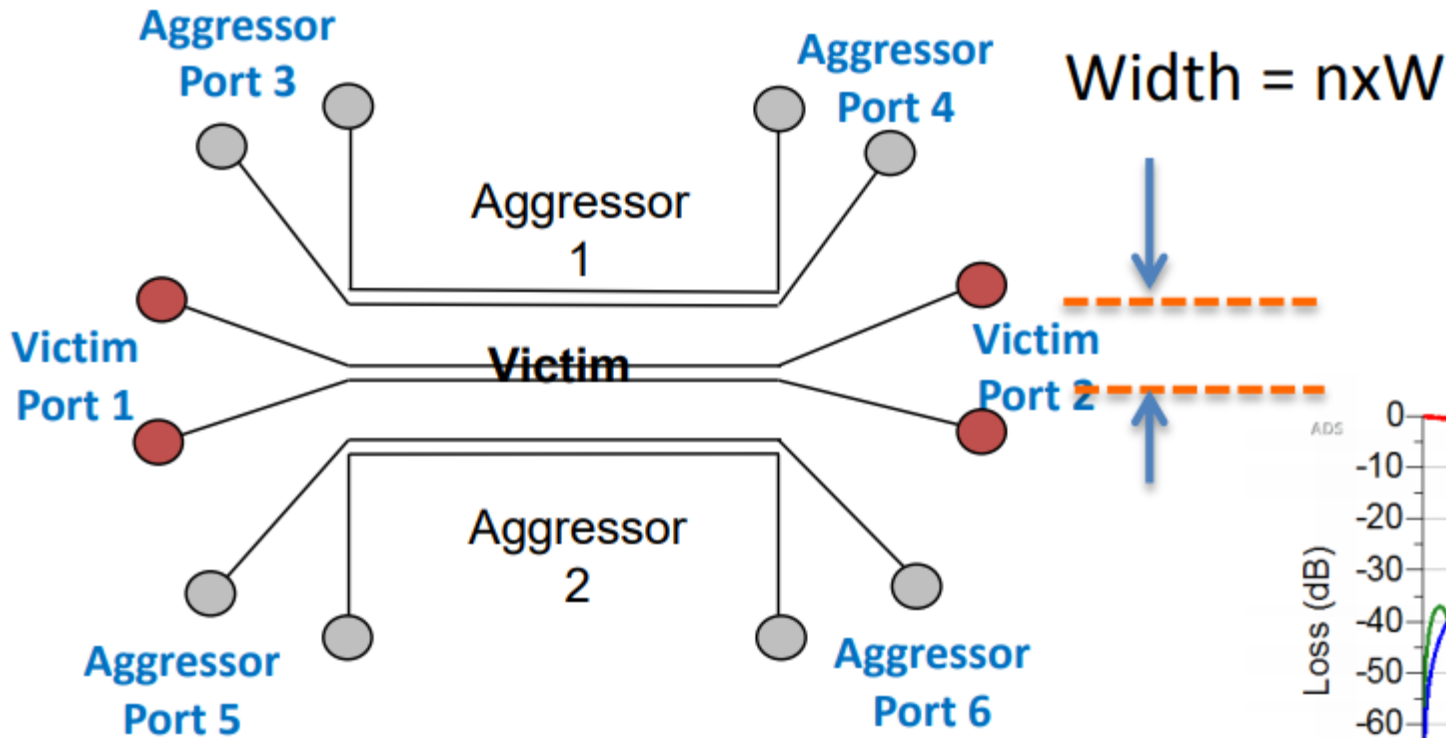
$$\text{Integrated return loss: } IRL = \sqrt{\frac{\int_0^{f_m} |V_{in}(f)|^2 |S_{21}(f)|^2 (|S_{11}(f)|^2 + |S_{22}(f)|^2) df}{\int_0^{f_m} |V_{in}(f)|^2 df}}$$

$$\text{Integrated insertion loss: } IIL = \sqrt{\frac{\int_0^{f_m} |V_{in}(f)|^2 |S_{21}(f)|^2 df}{\int_0^{f_m} |V_{in}(f)|^2 df}}$$

$$\text{Integrated crosstalk: } ITX = \sqrt{\frac{\int_0^{f_m} |V_{in}(f)|^2 \sum_{i \neq j} |S_{ij}(f)|^2 df}{\int_0^{f_m} |V_{in}(f)|^2 df}}$$

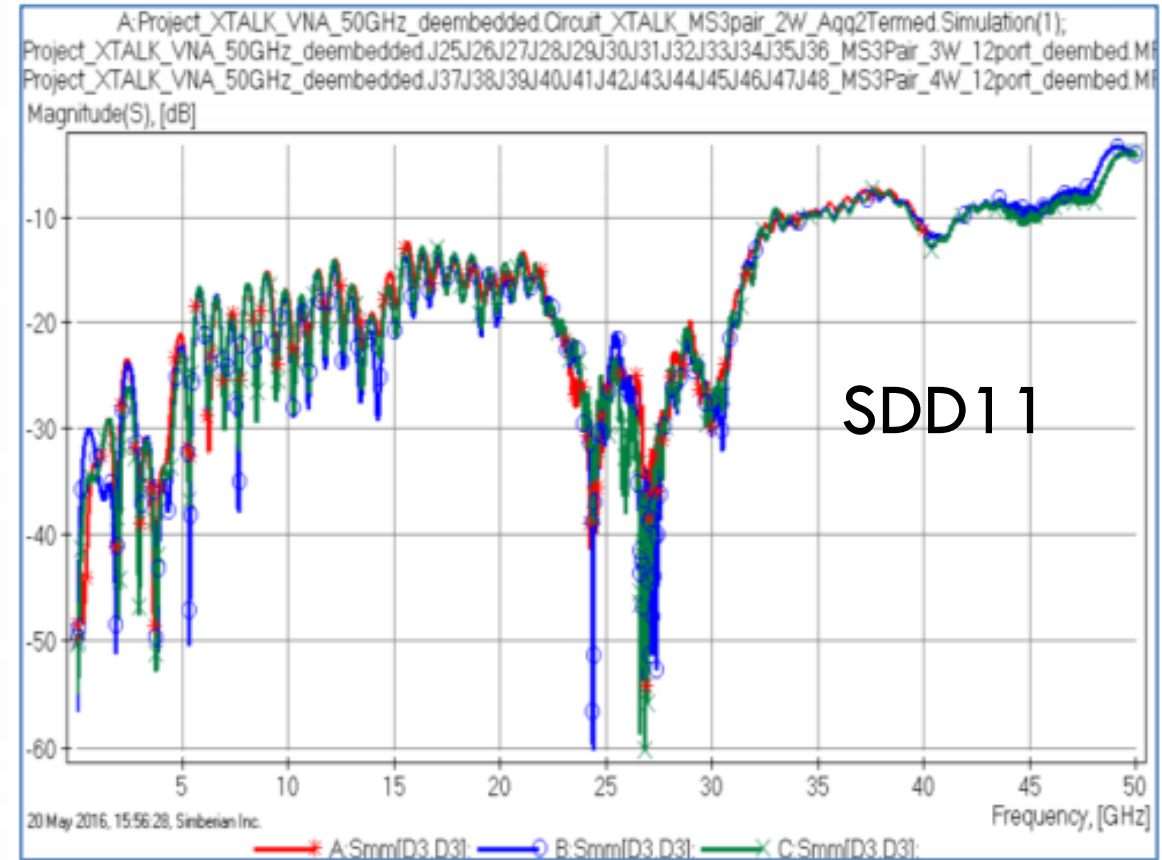
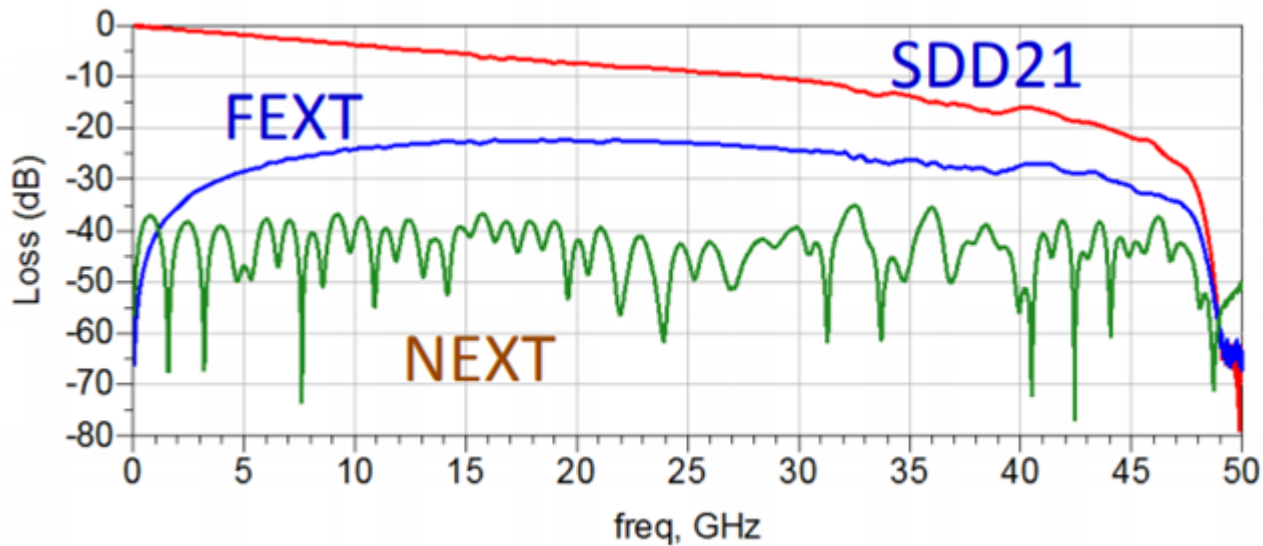
# • Neves et al. "Pathological Design", 100GBase-KR

- Decrease width, .5W, 1W, 2W, 4W, and 5W, translates to less crosstalk.
- 4, and 5W would be used with other high loss structures
- Each structure is optimized for same SDD11.

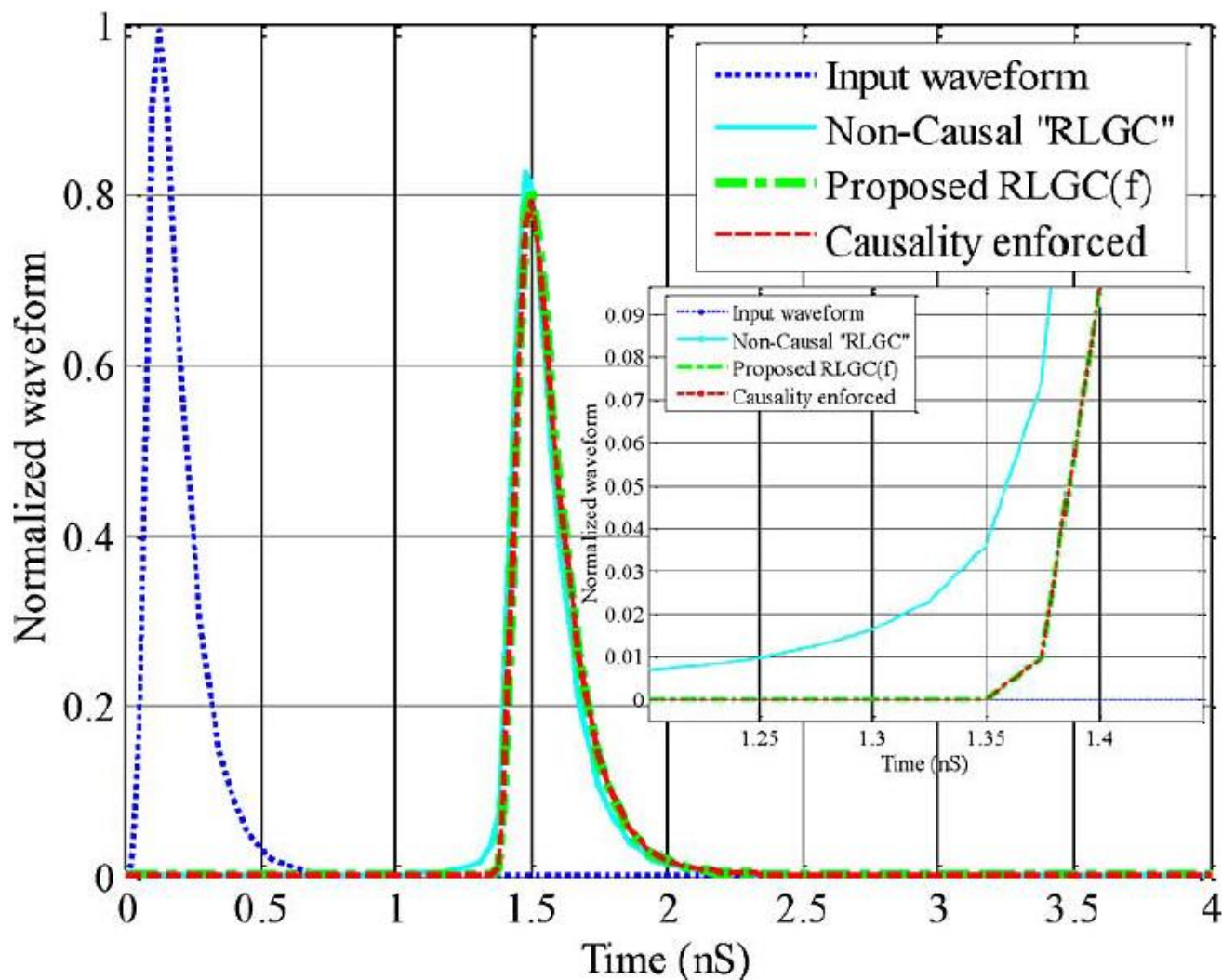


# • Neves et al. "Pathological Design", 100GBase-KR

- Measure SDDx1 (FEXT/NEXT) for given SDD11
- Iterate through geometry

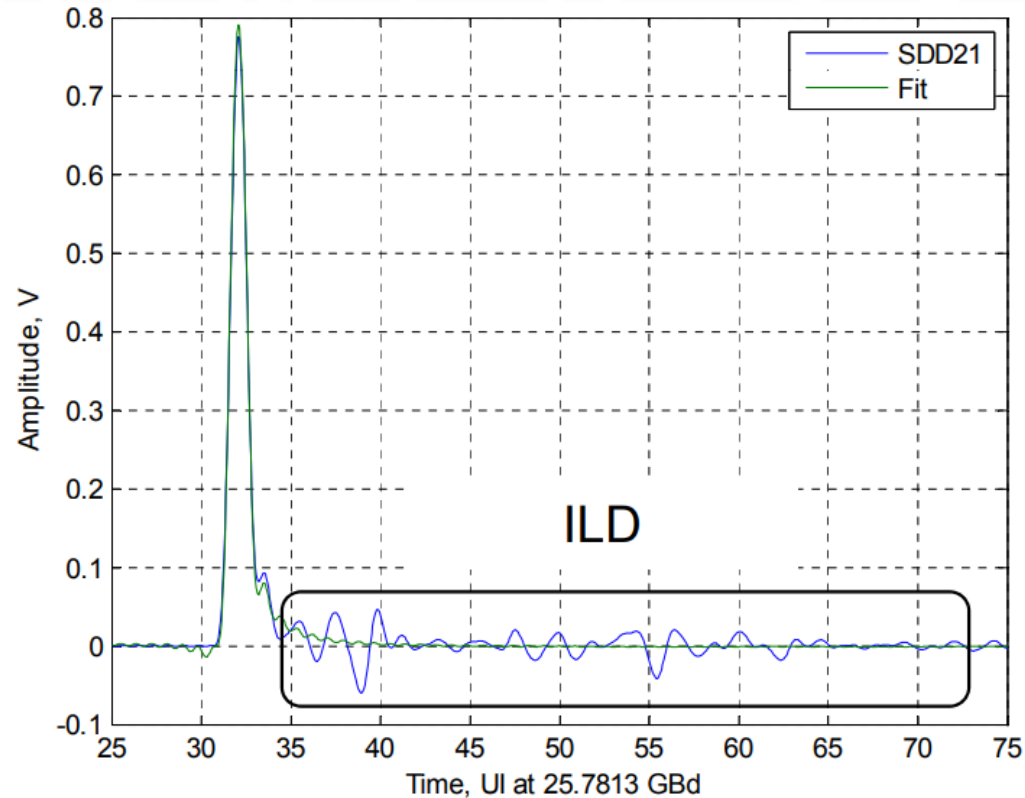


- **Zhang et al.: Model extraction**
- Input S-parameter and impulse response measurement, extract geometric trends
- Extract transmission line values ( $L_\infty, R_S, R_{DC}, K_g, \epsilon_R, \epsilon_I$ )
- Problems:
  - Copper roughness included in  $R_S$
  - Overly complicated algorithm



# Empirical Design: Evaluation

- Useful to compare with some benchmark → Impulse response
- Example under IEEE P802.3bj and P802.3ba models



$$H = e^x$$

$$\log(H_{fit}) = x \cong \gamma_0 + \gamma_1\sqrt{f} + \gamma_2f + \gamma_4f^2$$

$$\gamma_i = \alpha_i + j\beta_i$$

$$H_{ild} = H - H_{fit}$$

Minimization  
objective



# Numerical Methods

- **A.k.a. Design Exploration**

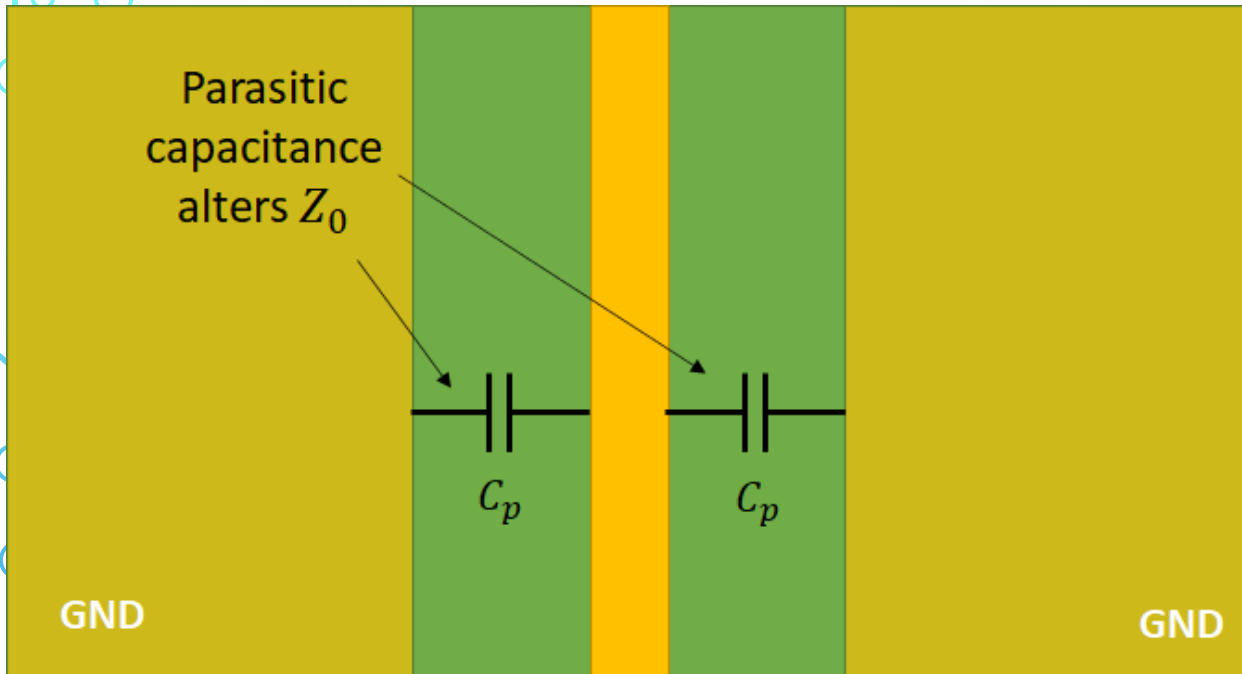
- Objective function: Signal integrity (S/Z-parameters), possibly EMI
- Design variables: Channel geometry
- Parameters: Roughness, Dk/Df, stack-up, etc.

- **Procedure:** Generate objective, iterate through variable range, build design space

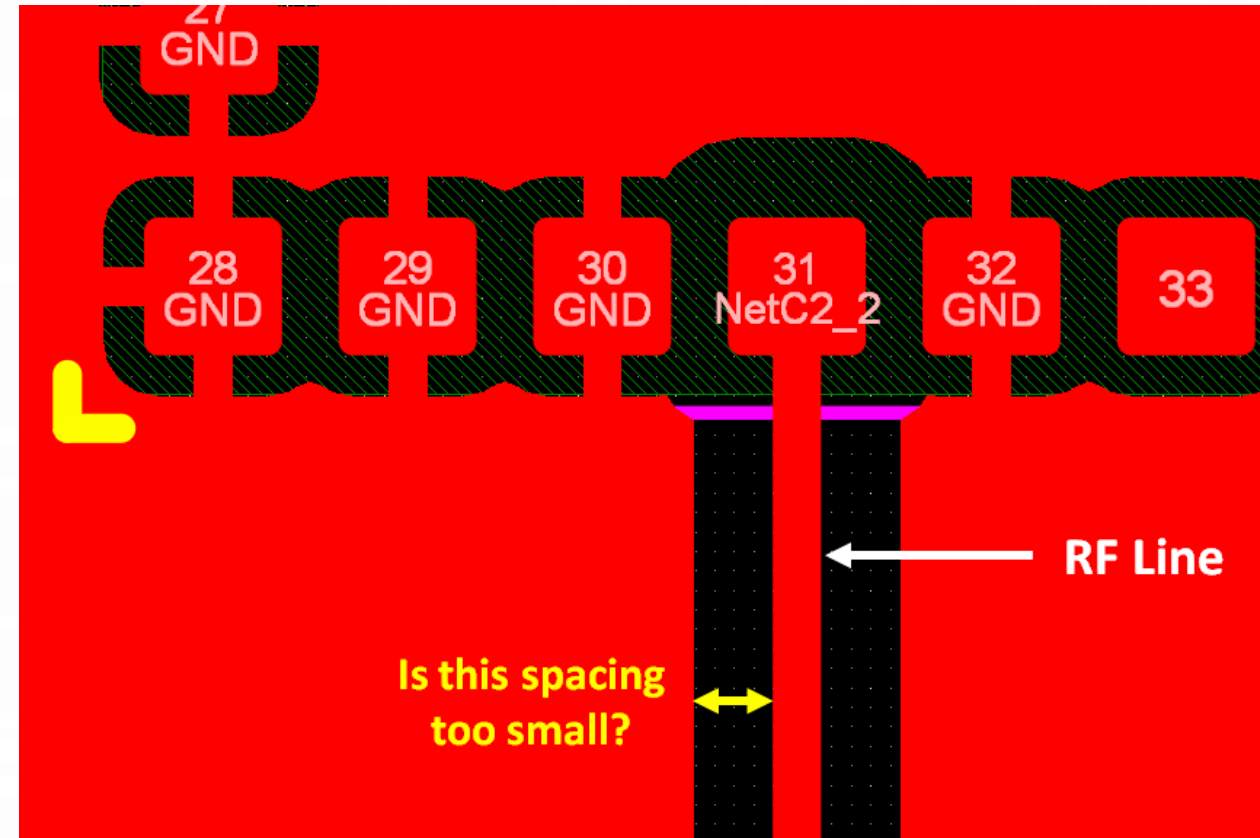
- **Drawbacks:** Requires finished or proposed layout, slow!

# Example: Copper Pour Clearance Constraints

- What's the allowed pour clearance near controlled impedance traces?



$$Z_0 = \sqrt{\frac{L}{C_{total}}} = \sqrt{\frac{L}{C + 2C_p}}$$



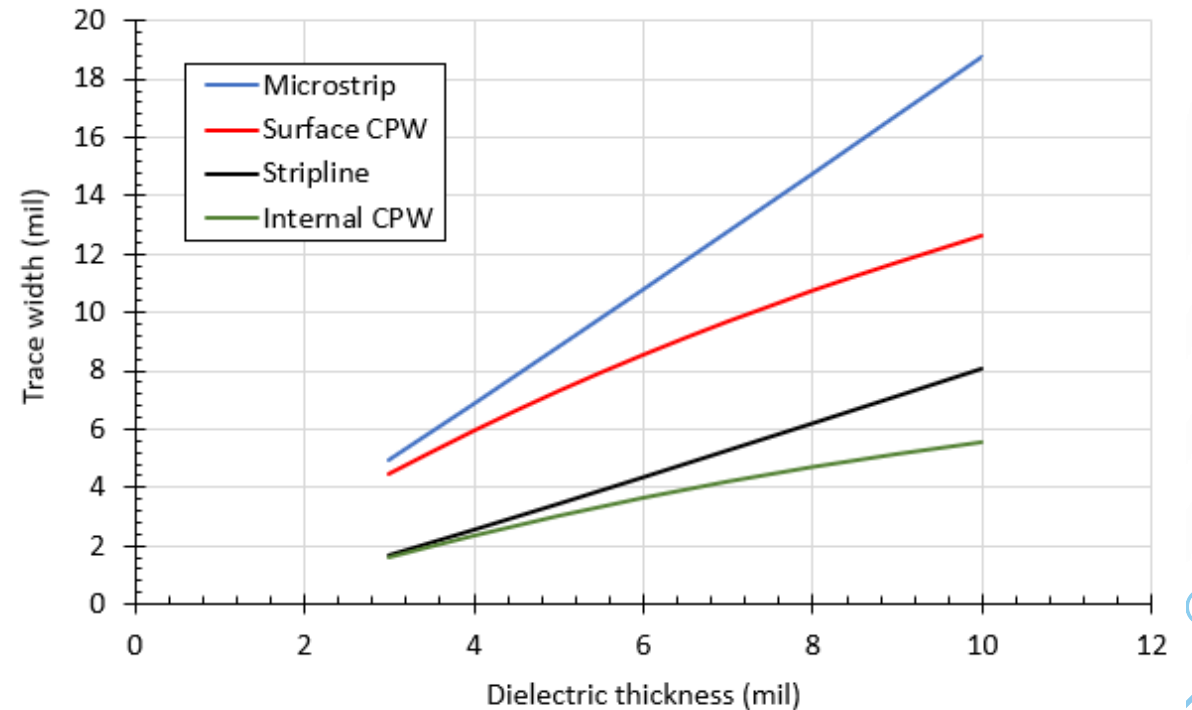
# Problem Statement

- What's the smallest allowed clearance?

$$\min \left[ \int_{\omega_1}^{\omega_2} |Z(\omega) - Z_{target}|^p d\omega \right]^{1/p}$$

$$\text{s.t.: } \begin{aligned} W &> 0 \\ S &> 0 \\ T &\in \{T_i\} \\ H &\in \{H_i\} \end{aligned}$$

Trace width for 50 Ohm impedance, 5 mil clearance

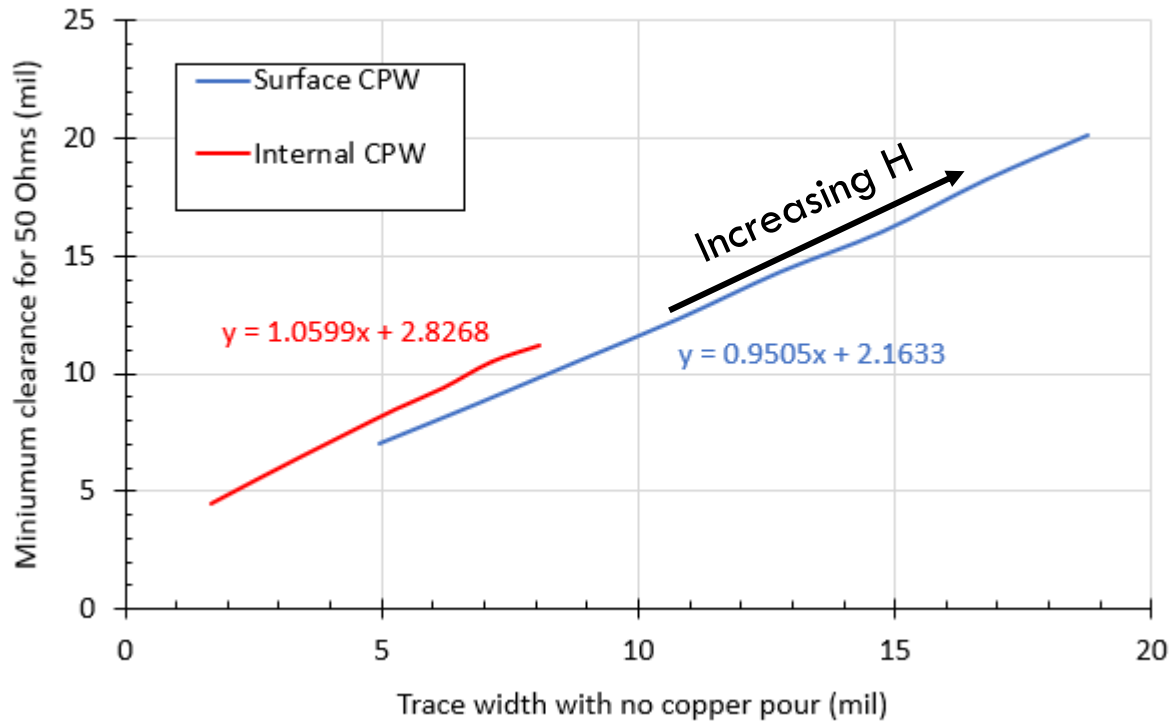


- Determine curve relating CPW with non-CPW

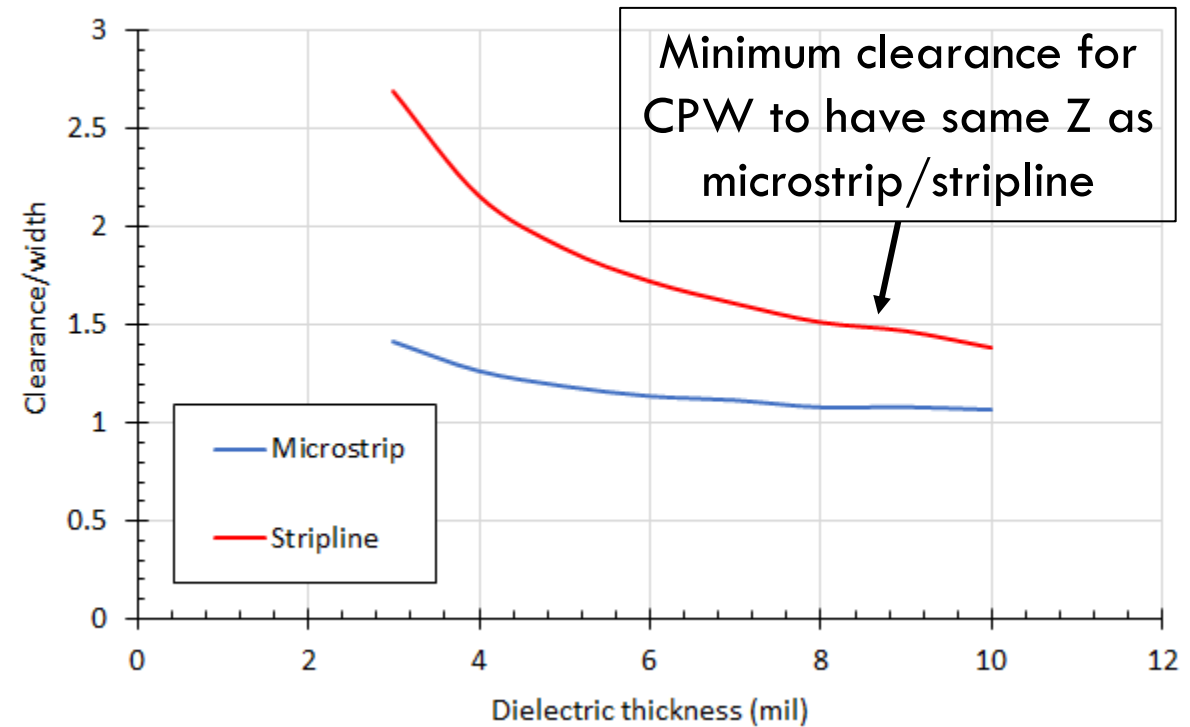
# Accidentally Testing “Rules of Thumb”

- We can easily violate the “3W” clearance rule without affecting impedance

Clearance required for matching trace width

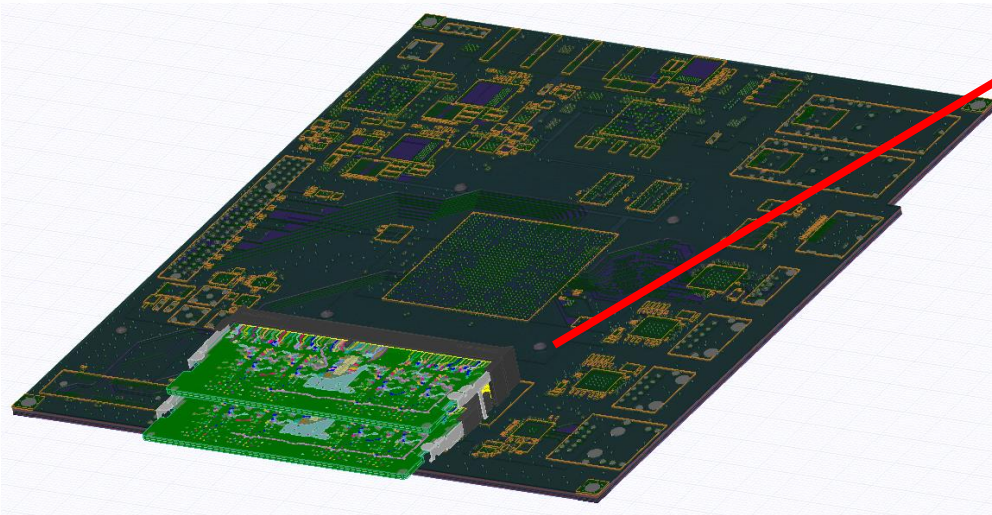


“3W” rule test for 50 Ohm impedance

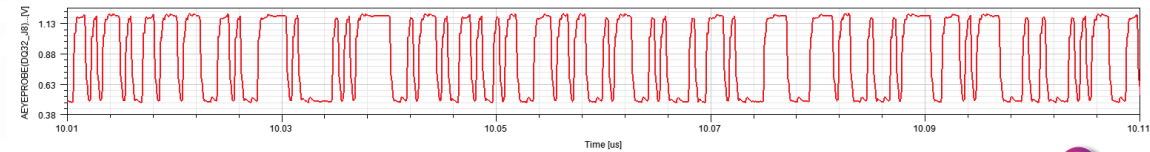
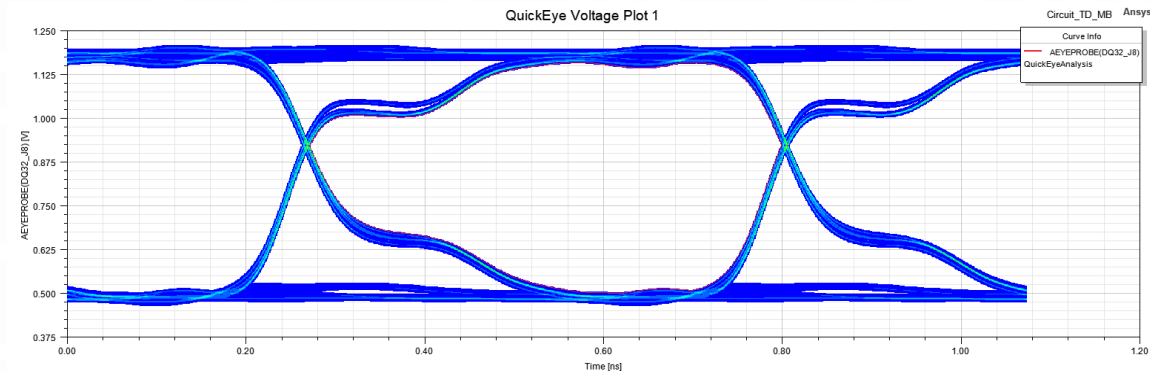
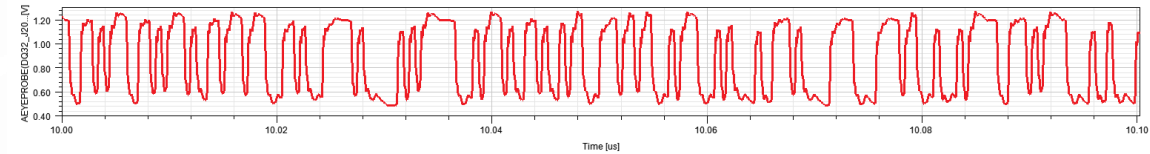
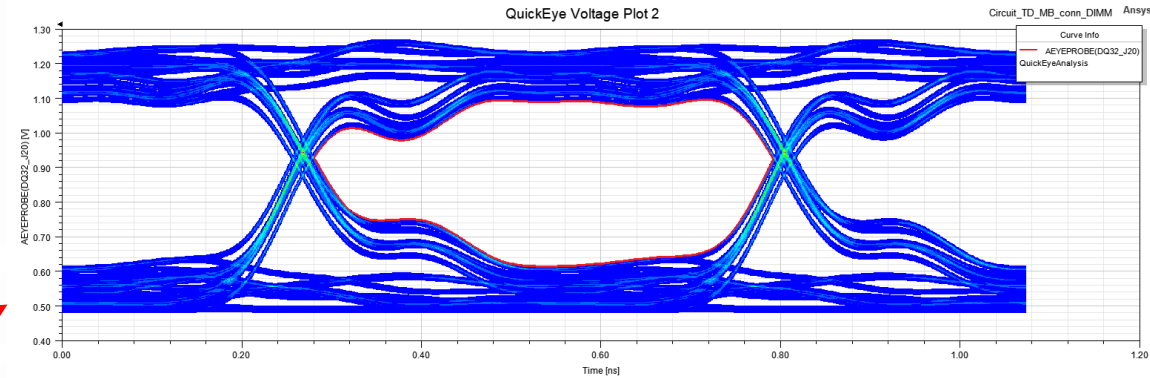


# Broader Trend: Design Exploration

- **Example: DDR SODIMM connectors**



Swap connectors or change stackup to get past 1866 MHz



# Analytical Methods

- **Deriving analytical models**

- Objective function: Signal integrity (S/Z-parameters), possibly EMI
- Design variables: Channel geometry
- Parameters: Roughness, Dk/Df, stackup, etc.

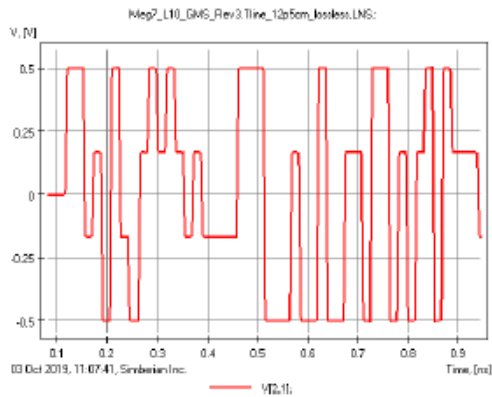
- **Procedure:** Calculate objective directly, optimize for geometry and dispersion

- **Drawbacks:** Difficult to consider parasitics and complex layouts

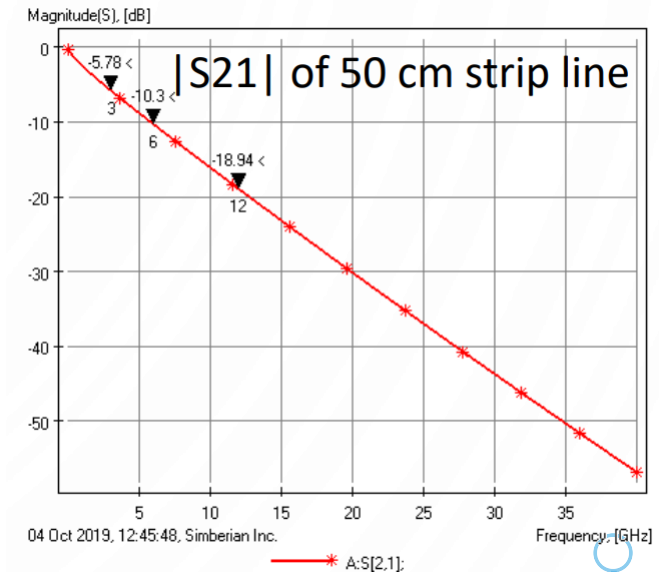
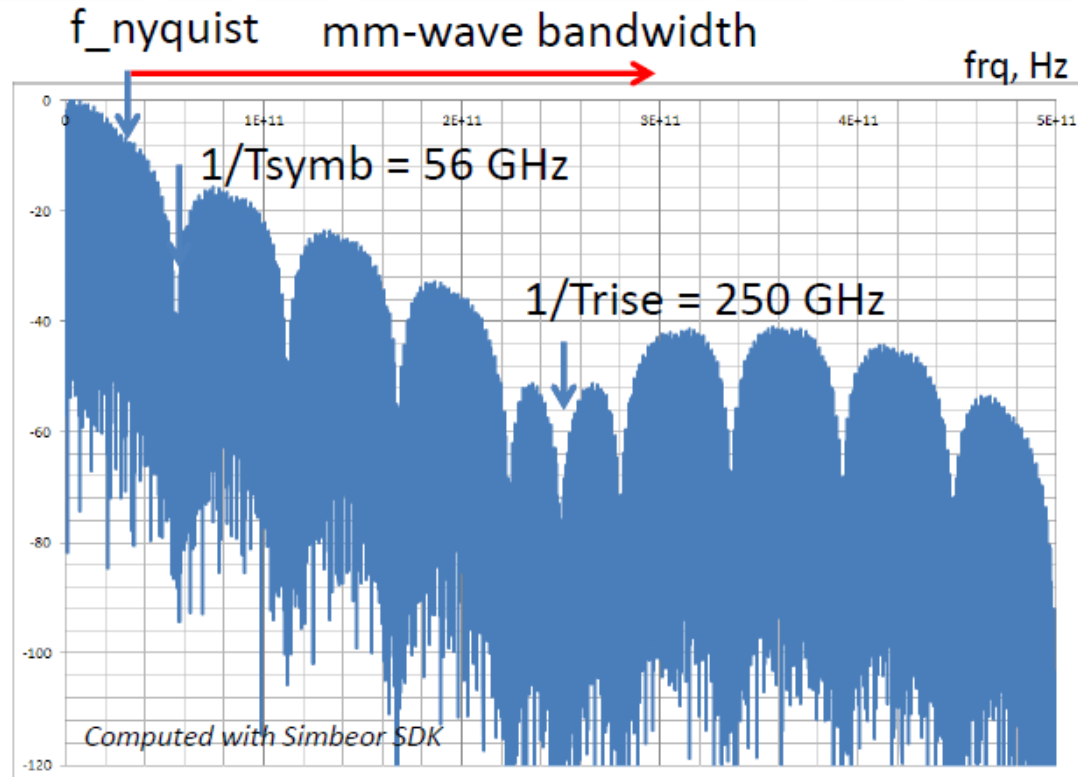
# Analytical: Wideband Interconnect Design

- **Example: 112 Gbps PAM4 signaling**

112 Gbps: Trise=4ps;  
 Tsymb=17.8571ps;  
 $f_{nyquist} = 28 \text{ GHz}$



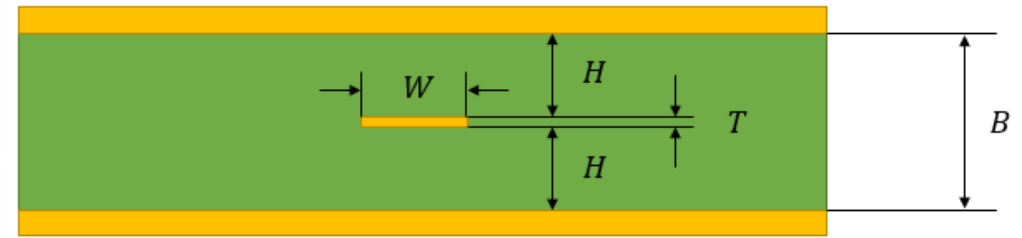
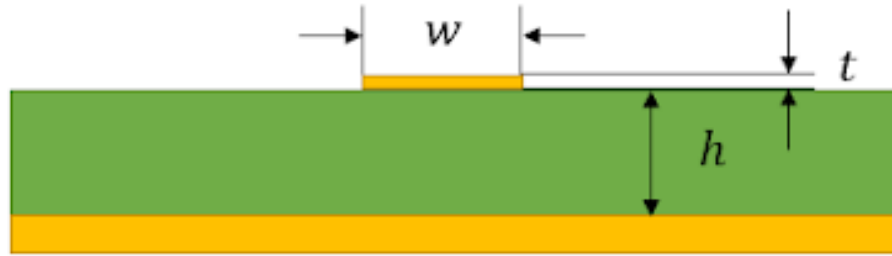
PSD of PRBS7



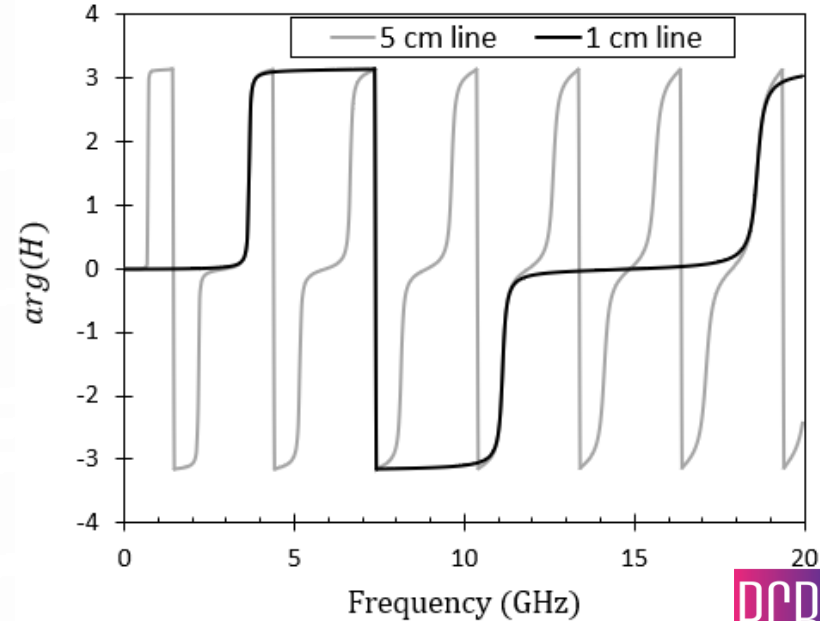
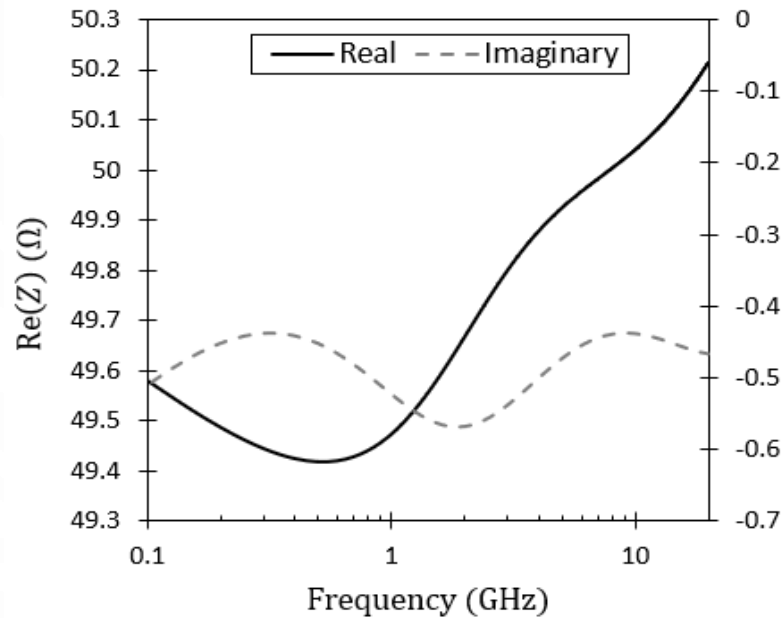
What is the bandwidth?  
 0.5/Trise looks unrealistic...

# Interconnect Optimization

- Many parameters: geometry, via count, length,...



- Allowed impedance mismatch, dispersion, crosstalk...





# Transmission Line Optimization: RLCG model

- TL characteristic impedance:  $Z_0 = \sqrt{\frac{R+i\omega L}{G+i\omega C}}$

$$R(\omega) = R_{DC} + \sqrt{\omega}R_s \quad L(\omega) = L_\infty + \frac{R_s}{\sqrt{\omega}}$$
$$G(\omega) = \omega C(\omega) \tan \delta(\omega) \quad C(\omega) = K_g \epsilon_R(\omega) \epsilon_0$$

- Dielectric constant:  $\epsilon = \epsilon_R(\omega) + i\epsilon_I(\omega)$ ,  $\tan \delta = \frac{-\omega \epsilon_I(\omega) - \sigma_{sub}}{\omega \epsilon_R}$
- Need causal models or data for:

**Dielectric constant:**  $\epsilon(\omega)$

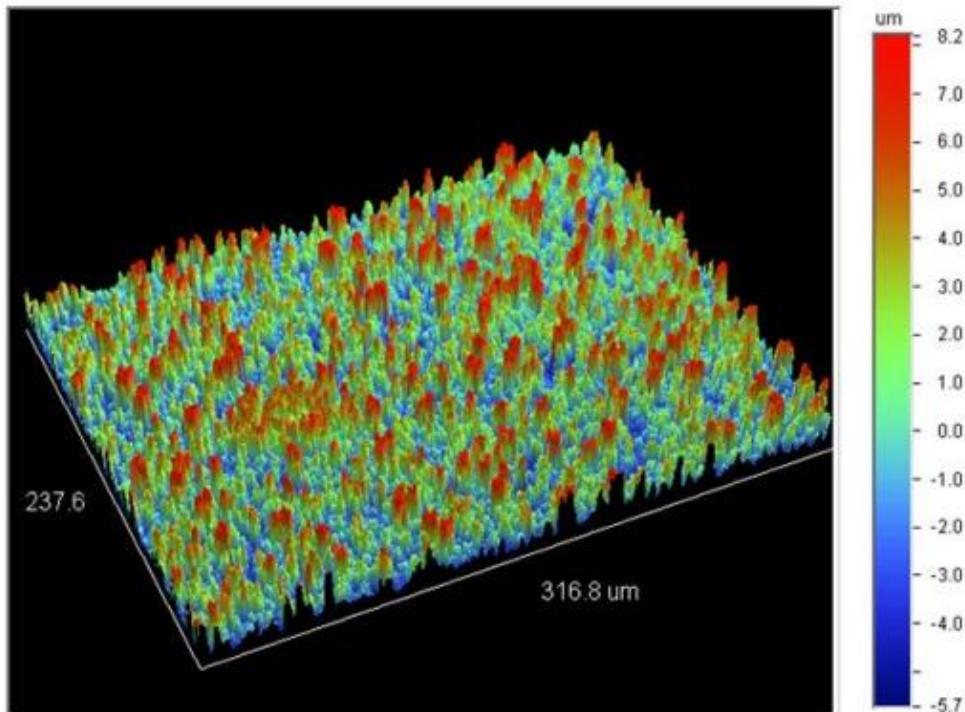
**Copper roughness:**  $K(\omega)$

**Electrical parameters:**  $R(\omega), L(\omega)$

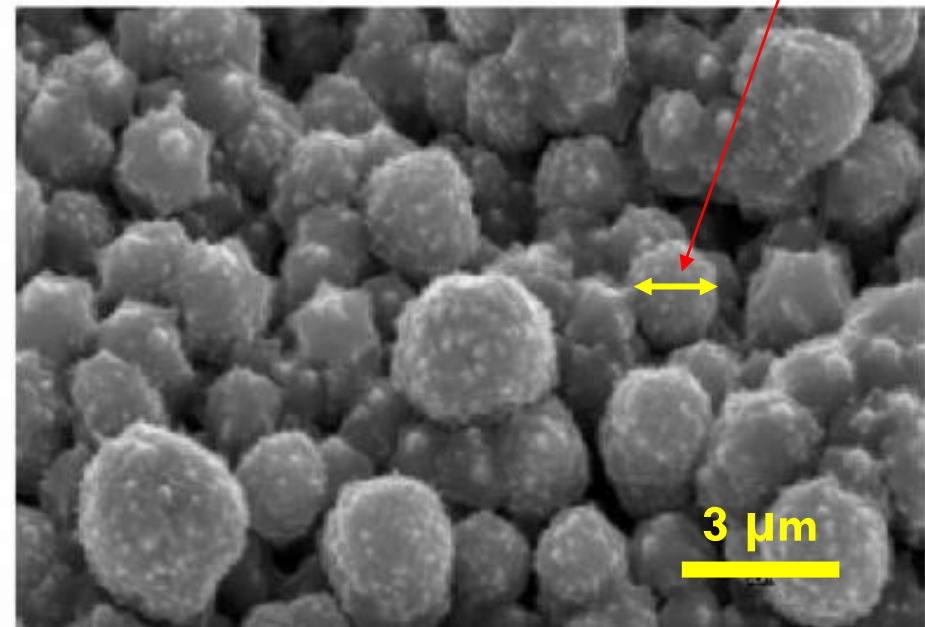
# Copper Roughness

- Copper roughness increases  $R_S$ : **non-resonant random scattering and absorption/relaxation**

$H_{RMS} \sim 5.6 \mu\text{m}$  on 2116 core



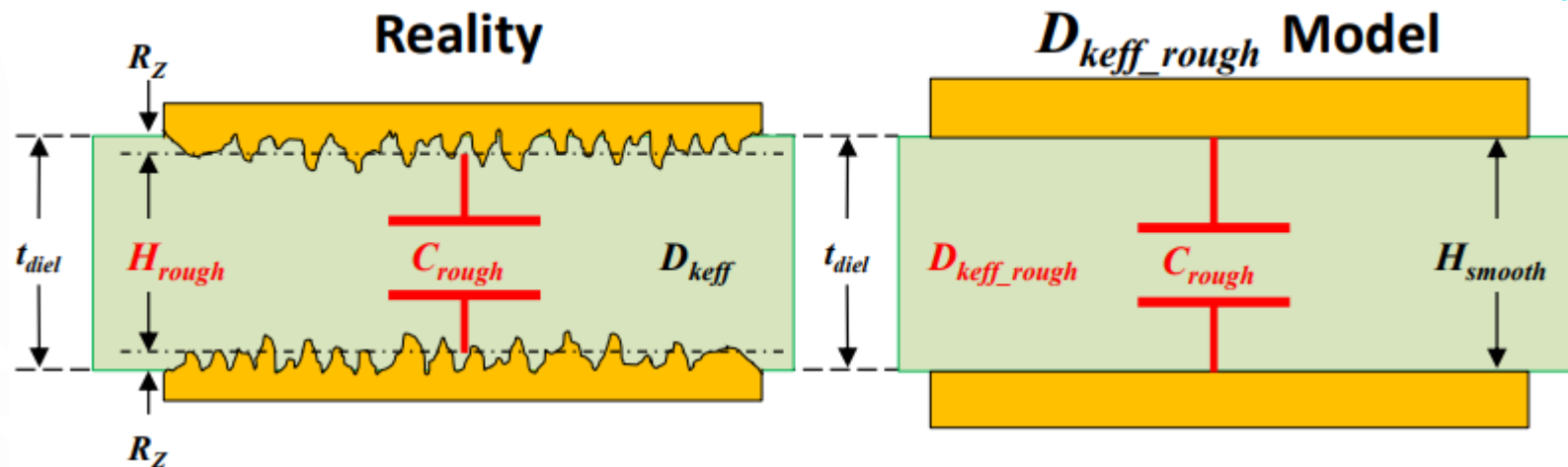
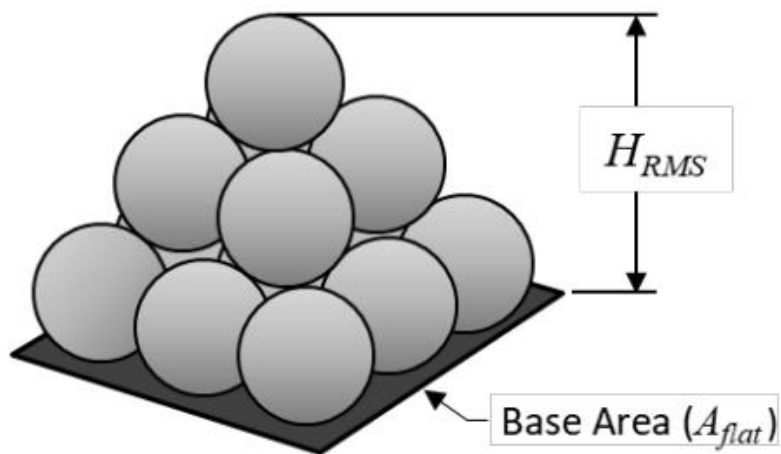
SEM image



Shlepnev, Y. "Practical methodology for analyzing the effect of conductor roughness on signal losses and dispersion in Interconnects," *DesignCon 2012*.

# Causal Copper Roughness Correction

- Cannonball-Huray (Other models: Hammerstad, Snowball Huray, etc.)



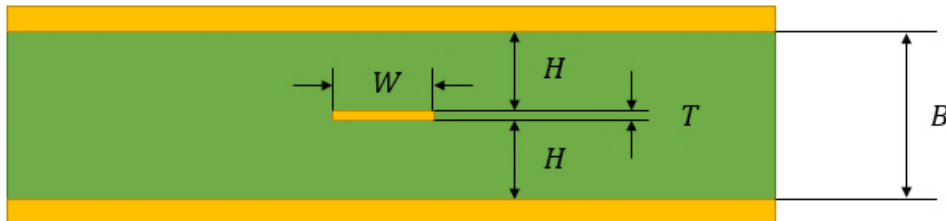
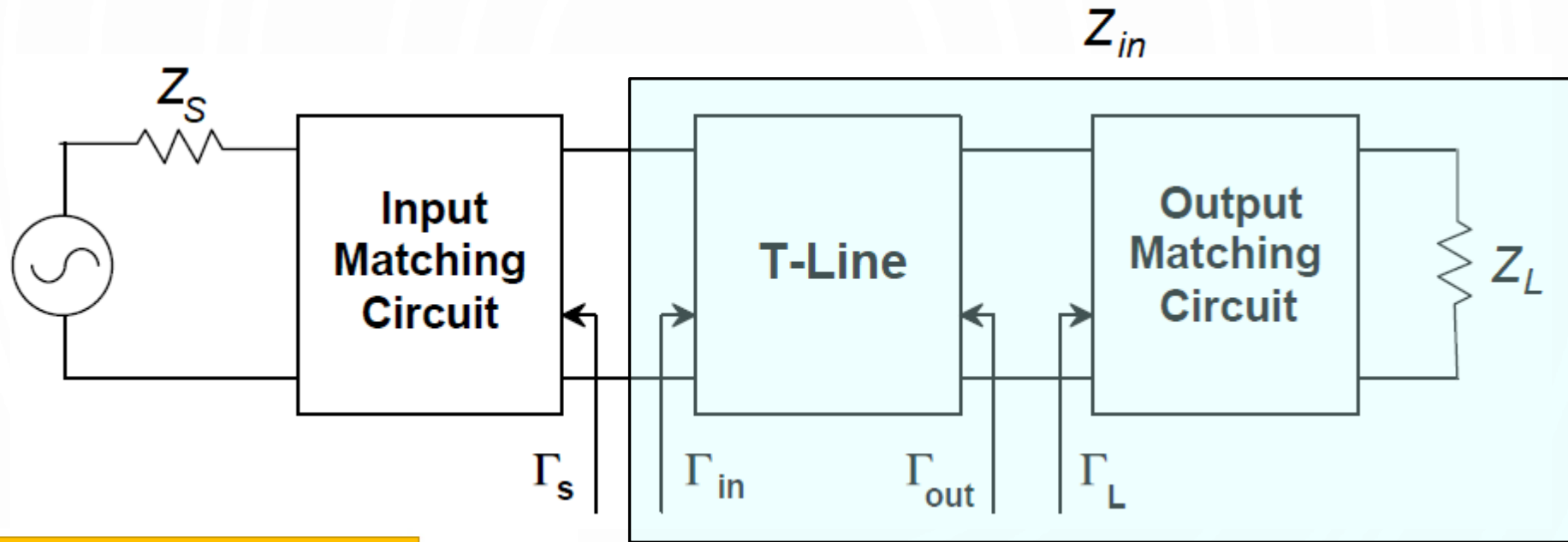
$$\varepsilon_c(\omega) = \varepsilon(\omega) \frac{t_{diel}}{t_{diel} - 2H_{10}}$$

$$R_s \rightarrow K(\omega)R_s$$

	Cannonball-Huray
Normalized frequency	$s = i\omega\mu_0\sigma a^2$ ( $a$ = cannonball radius)
Correction factor $K$	$1 + \frac{\sqrt{s}}{1 + \sqrt{s}}$

Dmitriev-Zdorov, V. "A Causal Conductor Roughness Model and its Effect on Transmission Line Characteristics," *Signal Integrity Journal*, November 2018.  
 Simonovich, B. "PCB Interconnect Modeling Demystified," *DesignCon 2019*.

# Stripline Problem



- Lorentzian Parameters for  $\epsilon$ :

$\epsilon_{s1}$	$\epsilon_{s2}$	$\epsilon_{\infty}$	$\tau_1$ (ps)	$\tau_2$ (ps)	$\sigma$ ( $\Omega^{-1}\text{m}^{-1}$ )
4.081	4.068	3.95	82.12	5.712	$5.81 \cdot 10^7$

- Single objective:  $\min L^2 |Z - Z_{target}|$

# Analytical Approach (Dispersion + Roughness)

- Start with Wadell's dispersion-less impedance formulas, use the definitions:

$$v^{-1} = k/\omega = \sqrt{L_{\infty} K_g \epsilon_0 \epsilon_{c,R}(\omega)} = \sqrt{\epsilon_{c,R}(\omega)} / c_0, \text{ and}$$

$$Z_0 = \sqrt{L_{\infty} / K_g \epsilon_0 \epsilon_{c,R}(\omega)}$$

- Use N-pole Lorentzian model for  $\epsilon_c(\omega) = \frac{\epsilon(\omega)H}{H-2H_{10}}$ , causal  $K(\omega)$

- Skin effect:  $R_s(\omega) = \sqrt{\frac{\mu_0}{\sigma A}} \left( \sqrt{1 + (\rho\omega\epsilon_0\epsilon(\omega))^2} + \rho\omega\epsilon_0\epsilon(\omega) \right)^{-\frac{1}{2}} \approx \sqrt{\frac{\mu_0}{8\sigma(T+W)^2}}$

# Analytical Approach (Dispersion + Roughness)

- Include losses with linear transformation:

$$L_{\infty} = Z_0 \sqrt{\epsilon_{c,R}(\omega)} / c_0, \text{ apply transformation:}$$

$$i\omega L_{\infty} \rightarrow \frac{i\omega Z_0 \sqrt{\epsilon_{c,R}(\omega)} + (R_{DC} + \sqrt{\omega}(1+i)R_S)c_0}{c_0} = i\omega L_{\infty} + R_{DC} + \sqrt{\omega}(1+i)R_S$$

- For capacitance,  $K_g \epsilon_0 \epsilon_{c,R}(\omega) = \frac{\sqrt{\epsilon_{c,R}(\omega)}}{Z_0 c_0}$ , apply transformation  $C \rightarrow G + i\omega C$

- Therefore,  $G + i\omega C = i\omega K_g \epsilon_0 \epsilon_{c,R}(\omega)(1 - i \tan \delta) = i\omega \frac{\sqrt{\epsilon_{c,R}(\omega)}}{Z_0 c_0} (1 - i \tan \delta)$

# Analytical Approach (Dispersion + Roughness)

- Define  $Z = \frac{i\omega L_\infty + R_{DC} + \sqrt{\omega}(1+i)R_s}{i\omega K_g \epsilon_0 \epsilon_{c,R}(\omega)(1 - i \tan \delta)}$

$$Z(\omega) = \sqrt{\frac{i\omega Z_0^2 \sqrt{\epsilon_{c,R}(\omega)} + Z_0 c_0 (R_{DC} + (1+i)K(\omega)R_s \sqrt{\omega})}{i\omega \sqrt{\epsilon_{c,R}(\omega)}(1 - i \tan \delta(\omega))}}$$

- Define  $\gamma = (i\omega L_\infty + R_{DC} + \sqrt{\omega}(1+i)R_s)(i\omega K_g \epsilon_0 \epsilon_{c,R}(\omega)(1 - i \tan \delta))$

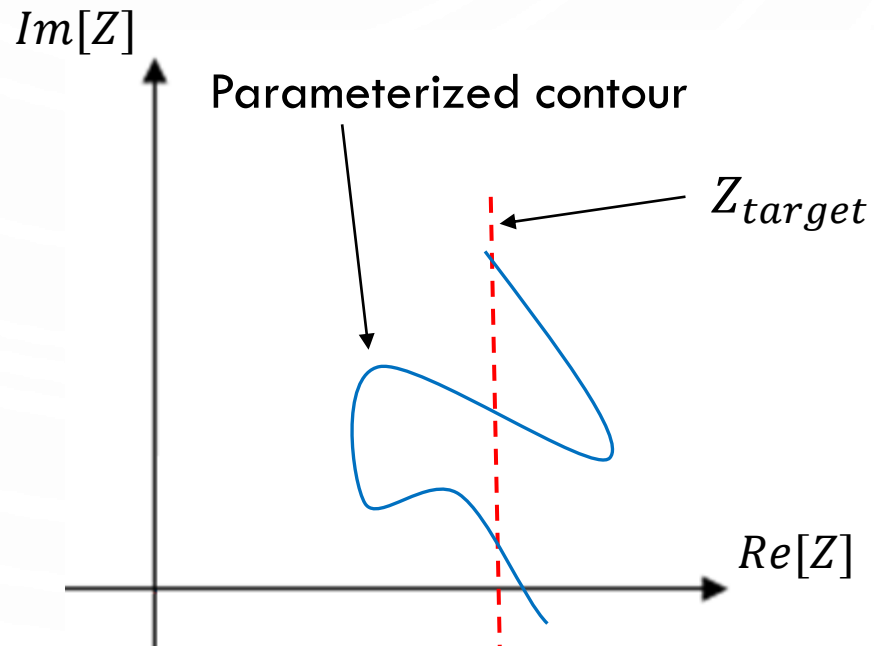
$$\gamma(\omega) = \sqrt{\frac{-\omega^2 Z_0 \epsilon_c(\omega) + i\omega c_0 \sqrt{\epsilon_{c,R}(\omega)}(1 - i \tan \delta(\omega))(R_{DC} + K(\omega)(1+i)\sqrt{\omega}R_s)}{Z_0 c_0^2}}$$

# Impedance Deviation Minimization

- Impedance is function of frequency  $\rightarrow$  **consider entire bandwidth**

- Use the  $L^p$  norm: 
$$\min \left[ \int_{\omega_1}^{\omega_2} |Z(\omega) - Z_{target}|^p d\omega \right]^{1/p}$$

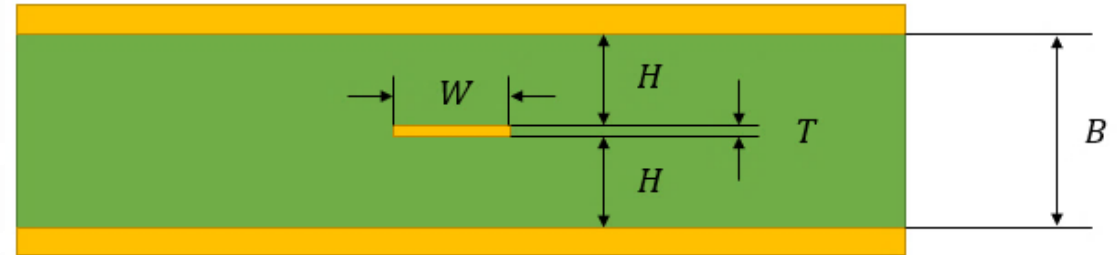
- For  $p = 2$ , equivalent to minimizing RMS deviation from a mean (target) value





# Example: Stripline Problem

- 8-layer stackup (equal layers),  
0.5 oz./ft.<sup>2</sup> Cu, 25 cm line  
 $H_{10} = 5 \mu\text{m}$ ,  $a = 2 \mu\text{m}$



- 50 Ohm target, 1 pF load capacitance
- Constraints:  $0 < W/H < 6$ ,  $T$  and  $H$  fixed to stackup

- Lorentzian Parameters for  $\epsilon$ :

$\epsilon_{s1}$	$\epsilon_{s2}$	$\epsilon_{\infty}$	$\tau_1$ (ps)	$\tau_2$ (ps)	$\sigma$ ( $\Omega^{-1}\text{m}^{-1}$ )
4.081	4.068	3.95	82.12	5.712	$5.81 \cdot 10^7$

- Single objective:  $\min L^2 |Z - Z_{target}|$

# Optimization Algorithm (Single Objective)

**Input:**  $K, J, Z_T, N_{max}$

00. **While**  $N < N_{max}$

01. **Generate initial solution**  $Z(\omega)$  and  $W/H$  ←

Mutate w/ procedure  
in Storn & Price (1997).

02. **If**  $N < N_{max}$

03.     GenerateNew  $W'/H', Z'$

04.     **If**  $L^2 |Z'(\omega) - Z_T| < L^2 (Z(\omega) - Z_T)$

**and** ConstraintCheck = True ←

Check against constraints with  
method in Lampin (2002).

05.      $Z(\omega) = Z'(\omega), N = 0$

06.     **Go to 02**

07.     **Else**

08.     ConstraintMod ←

Select new  $Z(\omega)$  with  
method in Lampin (2002).

09.      $N \rightarrow N + 1$

10.     **Go to 04**

11. **Else**

12.     **End**

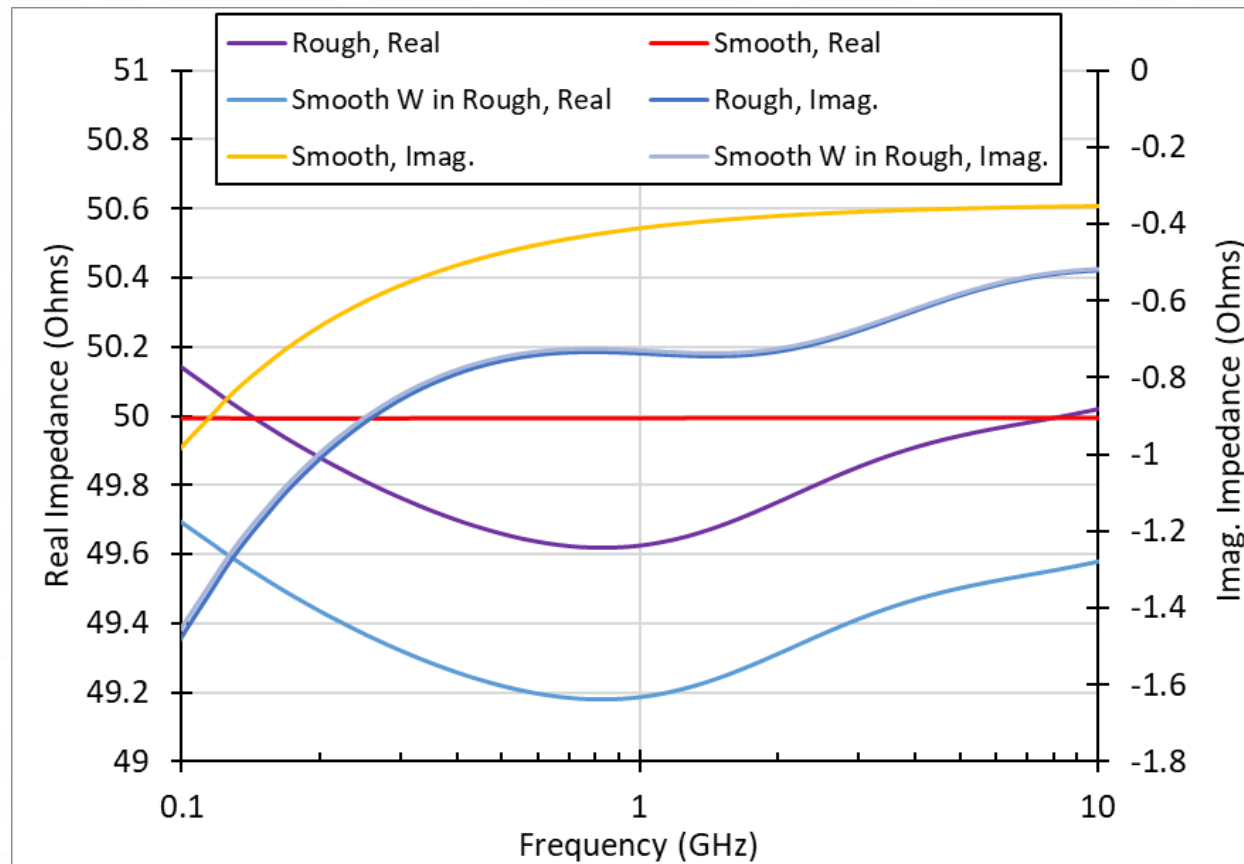
Storn, R., & Price, K. "Differential Evolution - A Simple and Efficient Heuristic for Global Optimization over Continuous Spaces," *Journal of Global Optimization*, 11, pp.341-359 (1997).

J. Lampinen, "A constraint handling approach for the differential evolution algorithm," *Proceedings of the 2002*

*Congress on Evolutionary Computation, CEC'02* (Cat. No.02TH8600), Honolulu, HI, USA, vol. 2, pp.1468-1473 (2002).

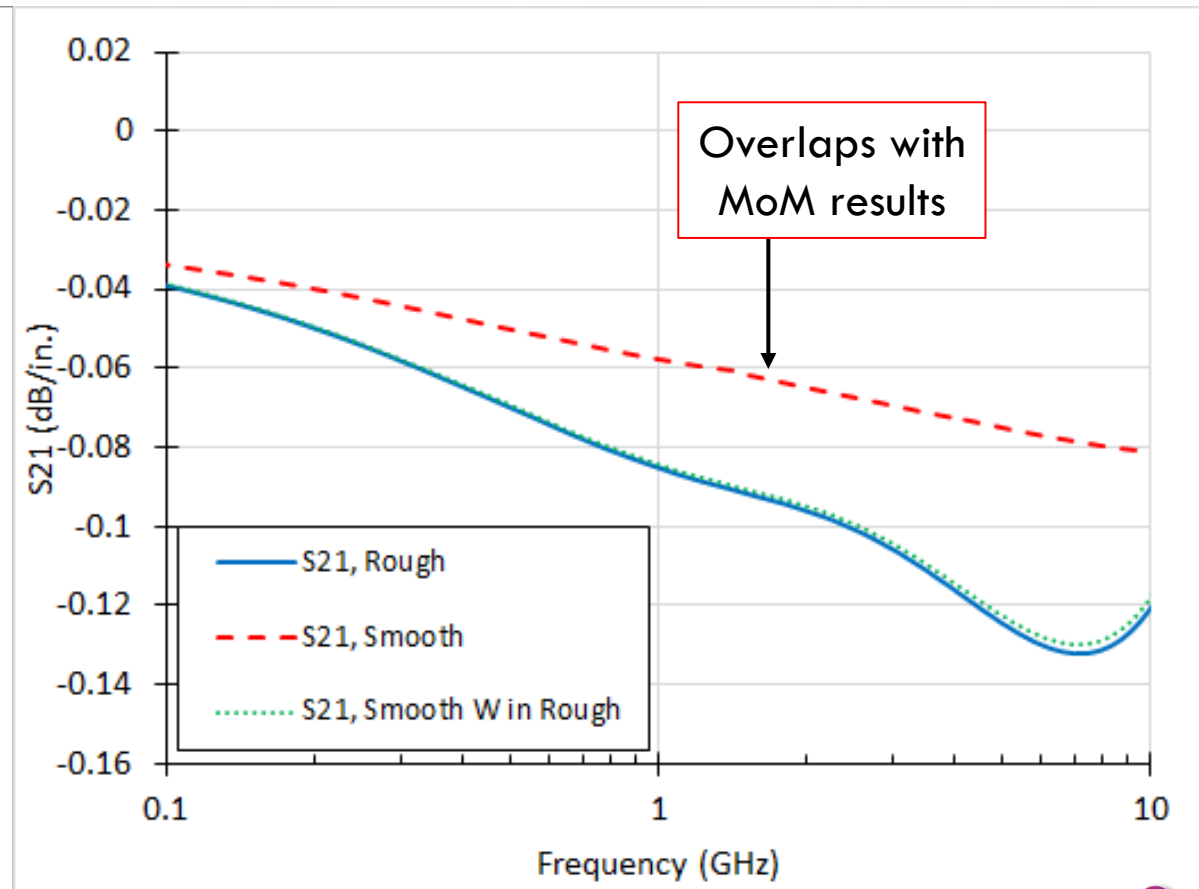
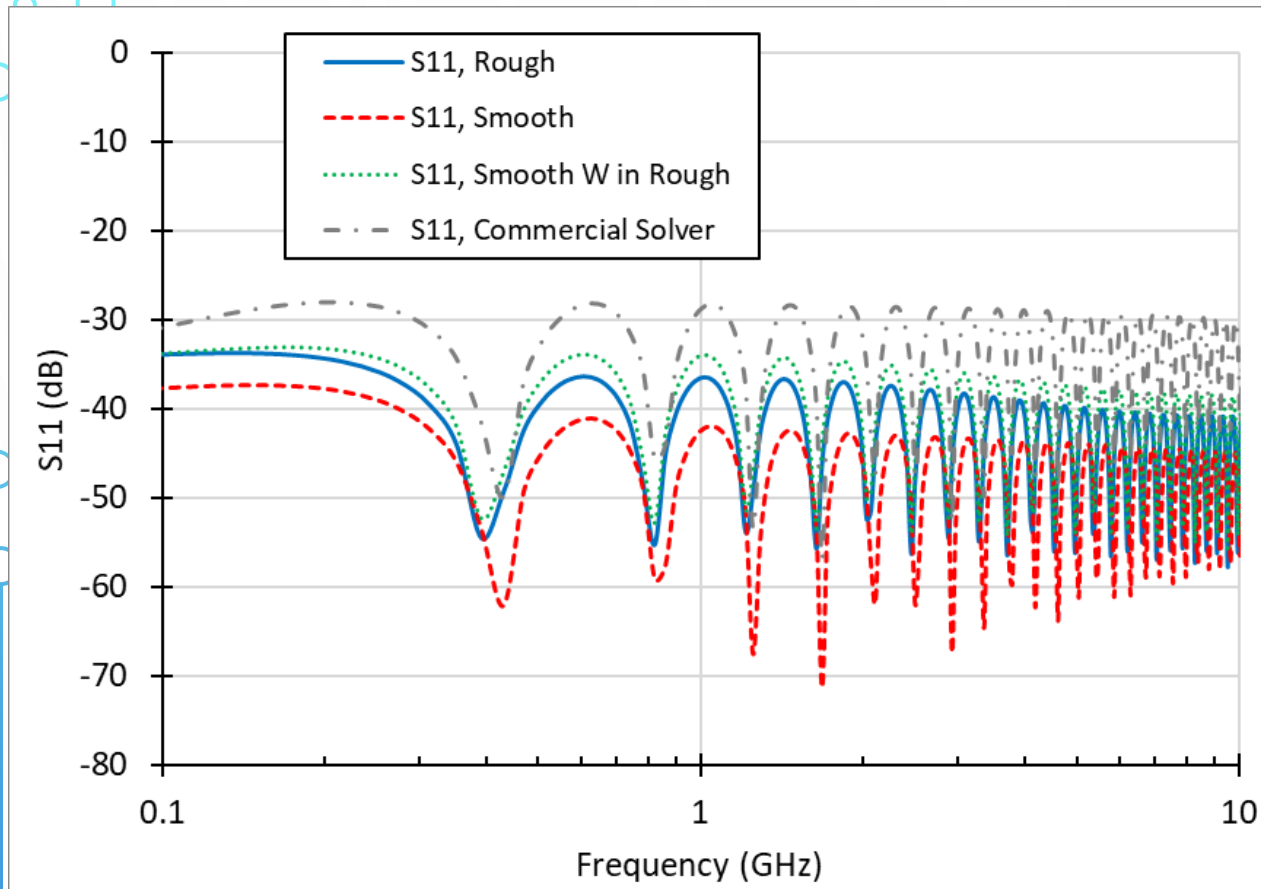
# Optimization Results

- Rough line:  $W = 0.178$  mm (6.996 mil)
- 50  $\Omega$  Smooth line:  $W = 0.180$  mm (7.085 mil)  $\rightarrow$  **No dispersion or skin effect**
  - Smooth dispersion-less line:  $\epsilon = 4.171 + 0.0576i$  (@ 1 GHz)
  - **Commercial MoM solver says 49.99 Ohms at 7.614 mils**



# Optimization Results

- Very similar return loss, very different insertion loss
- Note the commercial field solver results for return loss

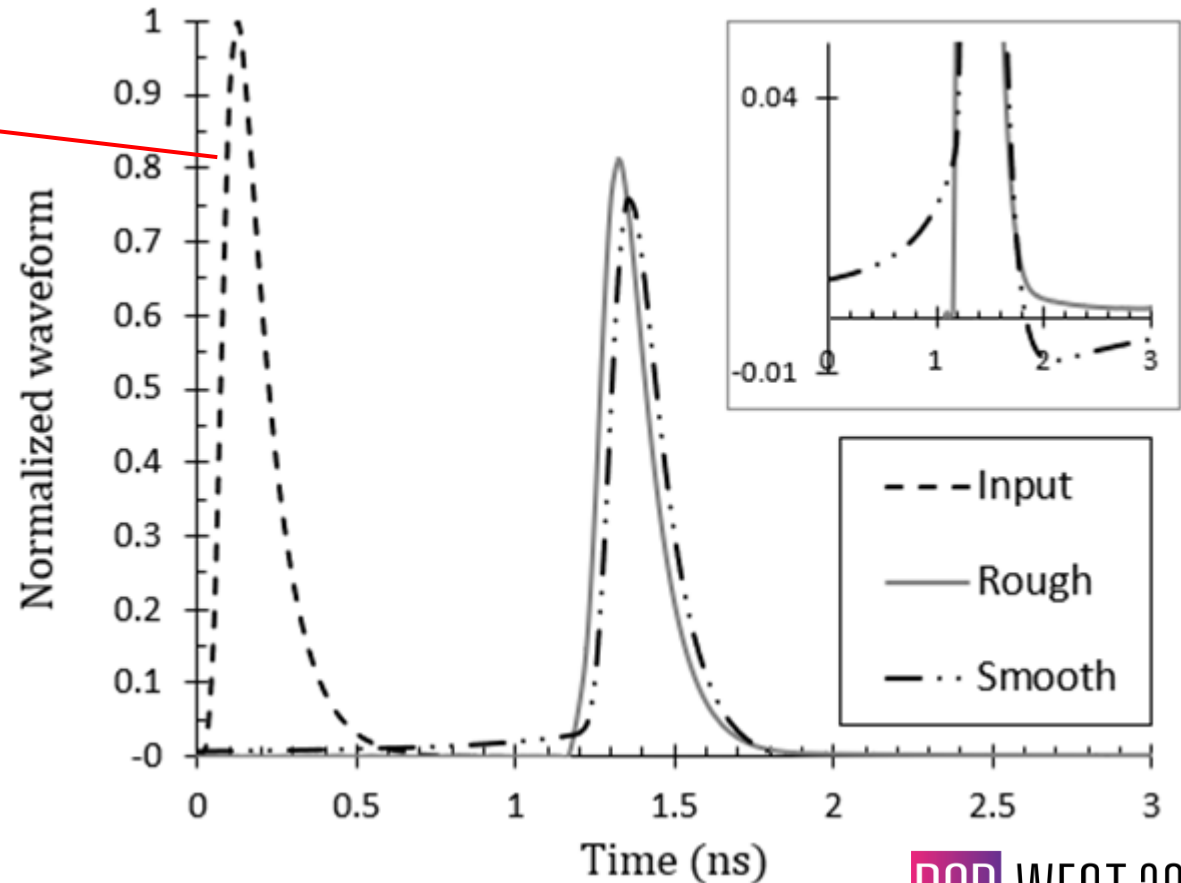


# Optimization Results - Causality

- Load capacitance arises in the line's transfer function
- Use a standard procedure for RLCG models to enforce causality (see ref.)

$$y(t) = \frac{10 \left(\frac{t}{\tau_0}\right)^4 e^{-\left(\frac{t}{\tau_0}\right)}}{1 + \left(\frac{t}{\tau_0}\right)^4}$$

1. Calculate transfer function  $H(\omega)$
2. Enforce causality to get  $H_c(\omega)$
3. Calculate  $h(t) = IFT[H_c(\omega)]$
4. Calculate  $h(t) * y(t)$

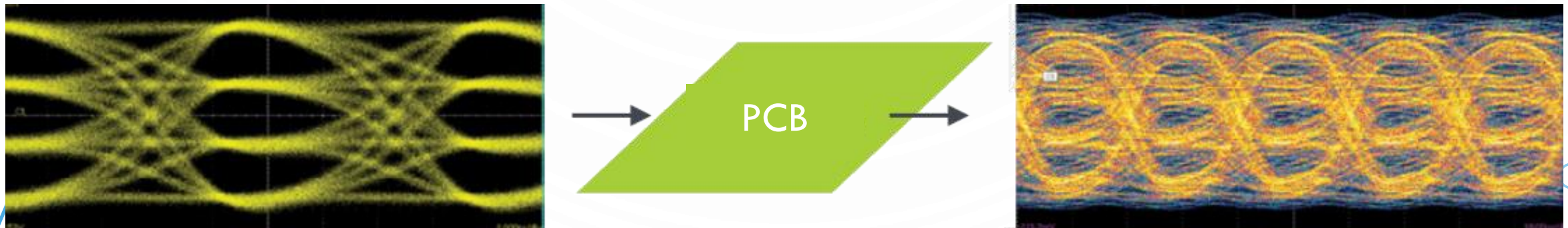


# Drawbacks

- Analytical models:
  - Difficult to account for things like differential impedance, fiber weave effects
  - Often need to incorporate numerical models
- Typically need to balance crosstalk, routing density, impedance control, and distortion → 4 objectives!
  - **Numerical model:** Wu, R.-B. and Yang, J.-C., “Boundary integral equation formulation of skin effect problems in multiconductor transmission lines,” *IEEE Transactions on Magnetics*, 25(4), 3013-3015 (1989).

# Looking Ahead

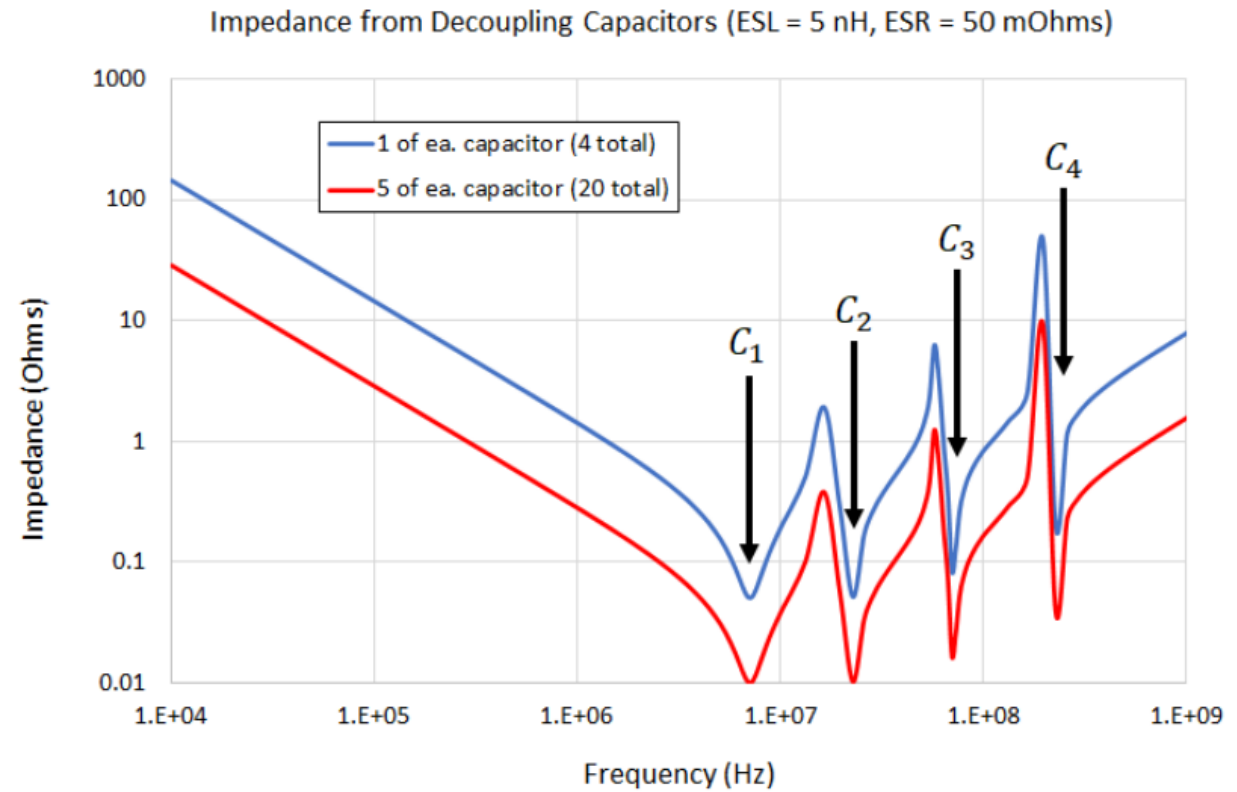
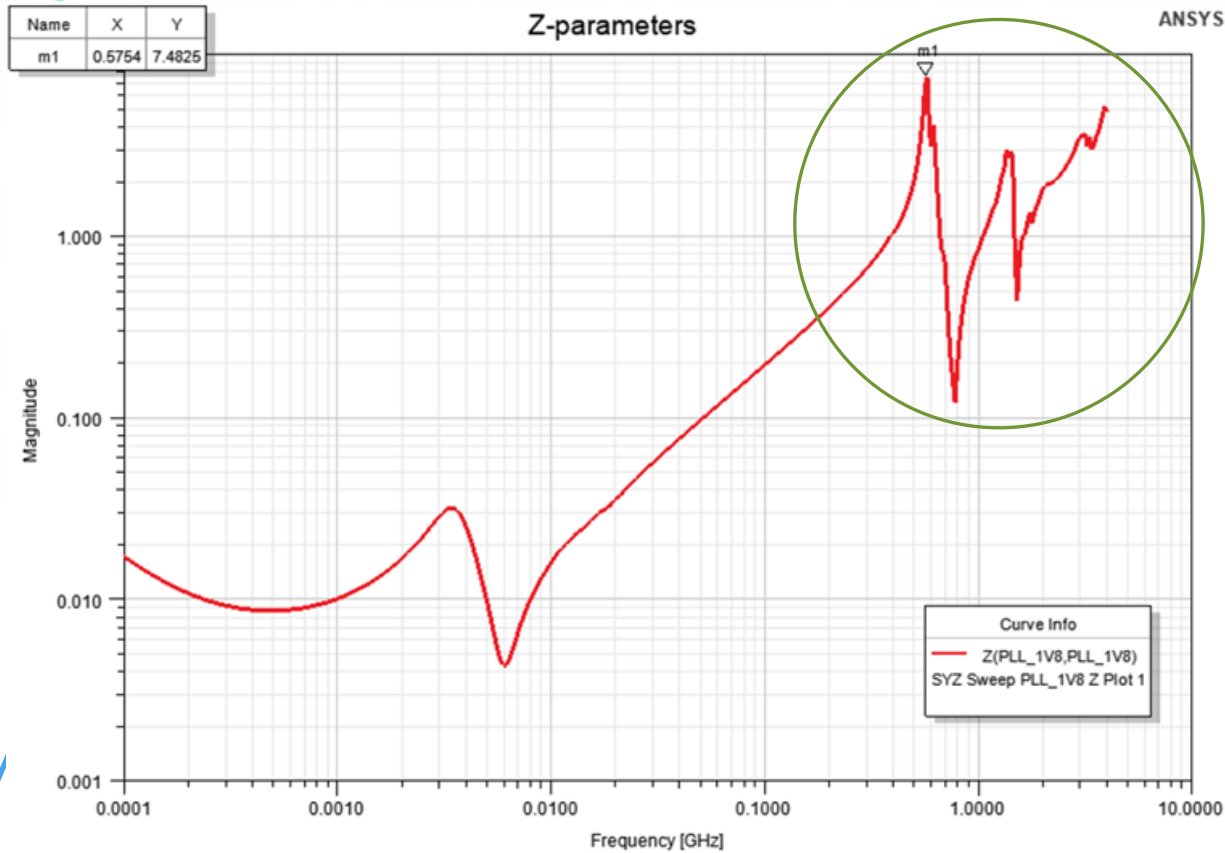
- Upcoming tech demands extremely precise interconnect designs
- **Examples:** 112+ Gbps PAM4, quantum computing, 5G/6G, radar, microwave photonics, IEEE 802.11ad (Multiple Gigabit Wireless System)



- **Constraints:** Insertion loss, ISI, crosstalk, impedance matching...

# Power Integrity

- Power integrity also critical in advanced designs



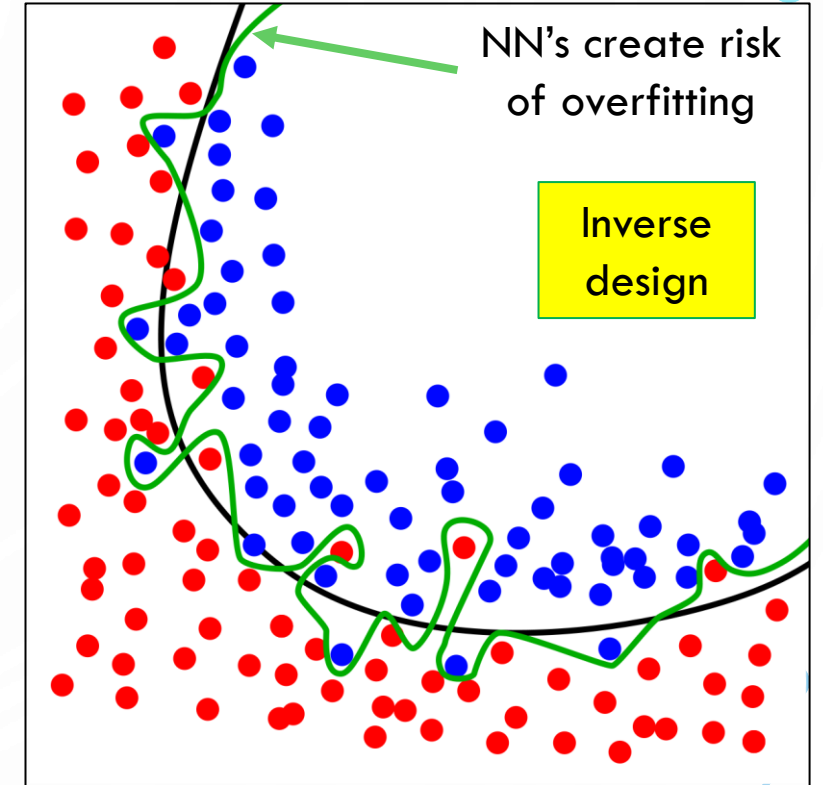


# Machine Learning in Interconnect Design

- ML models already being used for interconnect and device design:
  - Transmission lines/waveguides
  - Commercial 100 GHz-1 THz oscillators and interconnects
  - SerDes adaptive equalization
  - Power and thermal integrity (on-die, SiP, applies to boards)
  - Nanophotonics device design, including PICs
- Multivariate ML models for predicting  $Z$ , S-parameters,  $\gamma$ ,  $L$  &  $C$ ,  $H(\omega)$ , etc.

# Machine Learning in Interconnect Design

- Inverse design approach
- Optimization algorithms for specific systems and models
- Neural networks for prediction
  - Training  $\rightarrow$  build numerical model from measurements ( $Z, S, \gamma, K$  etc.)
  - Specific to routing topology, materials, geometry, manufacturing process etc...



THANK YOU!





Don't forget to complete your **session surveys** by accessing the PCB WEST Proceedings website. (An email containing the URL was sent to you this week.)

Once logged into the proceedings, access the surveys by choosing "Session Evaluations" and then "Select Sessions Attended."

Once completed, the professional development hours will be added to your certificate.

The **deadline** to complete surveys is **Nov. 8, 2021**.

Thank you!